

OptiMOS® Power-Transistor

Feature

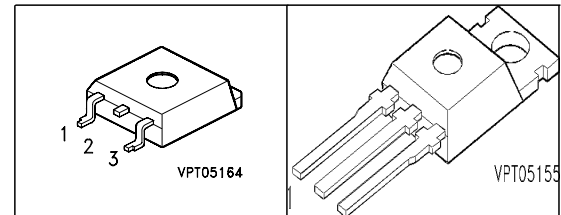
- N-Channel
- Enhancement mode
- Logic Level
- 175°C operating temperature
- Avalanche rated
- dv/dt rated

Product Summary

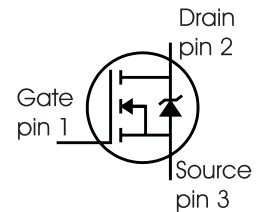
V_{DS}	55	V
$R_{DS(on)}$ max. SMD version	4.4	mΩ
I_D	100	A

P-TO263-3-2

P-TO220-3-1



Type	Package	Ordering Code	Marking
SPP100N06S2L-05	P-TO220-3-1	Q67060-S6043	PN06L05
SPB100N06S2L-05	P-TO263-3-2	Q67060-S6042	PN06L05



Maximum Ratings, at $T_j = 25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Value	Unit
Continuous drain current $T_C=25^\circ\text{C}$, ¹⁾ $T_C=100^\circ\text{C}$	I_D	100 100	A
Pulsed drain current $T_C=25^\circ\text{C}$	$I_{D \text{ puls}}$	400	
Avalanche energy, single pulse $I_D=80\text{A}$, $V_{DD}=25\text{V}$, $R_{GS}=25\Omega$	E_{AS}	810	mJ
Avalanche energy, periodic limited by T_{jmax}	E_{AR}	30	
Reverse diode dv/dt $I_S=100\text{A}$, $V_{DS}=44\text{V}$, $dI/dt=200\text{A}/\mu\text{s}$, $T_{jmax}=175^\circ\text{C}$	dv/dt	6	kV/ μs
Gate source voltage	V_{GS}	± 20	V
Power dissipation $T_C=25^\circ\text{C}$	P_{tot}	300	W
Operating and storage temperature	T_j , T_{stg}	-55... +175	$^\circ\text{C}$
IEC climatic category; DIN IEC 68-1		55/175/56	

Thermal Characteristics

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Characteristics					
Thermal resistance, junction - case	R_{thJC}	-	-	0.5	K/W
Thermal resistance, junction - ambient, leaded	R_{thJA}	-	-	62	
SMD version, device on PCB:	R_{thJA}				
@ min. footprint		-	-	62	
@ 6 cm ² cooling area ²⁾		-	-	40	

Electrical Characteristics, at $T_j = 25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static Characteristics					
Drain-source breakdown voltage $V_{GS}=0V, I_D=1mA$	$V_{(BR)DSS}$	55	-	-	V
Gate threshold voltage, $V_{GS} = V_{DS}$ $I_D =250\mu A$	$V_{GS(th)}$	1.2	1.6	2	
Zero gate voltage drain current $V_{DS}=55V, V_{GS}=0V, T_j=25^{\circ}C$ $V_{DS}=55V, V_{GS}=0V, T_j=125^{\circ}C$	I_{DSS}	- -	0.01 1	1 100	μA
Gate-source leakage current $V_{GS}=20V, V_{DS}=0V$	I_{GSS}	-	1	100	nA
Drain-source on-state resistance $V_{GS}=4.5V, I_D=80A$ $V_{GS}=4.5V, I_D=80A, SMD\ version$	$R_{DS(on)}$	- -	4.4 4.1	5.9 5.6	mΩ
Drain-source on-state resistance $V_{GS}=10V, I_D=80A$ $V_{GS}=10V, I_D=80A, SMD\ version$	$R_{DS(on)}$	- -	3.9 3.6	4.7 4.4	

¹Current limited by bondwire and calculated with max. source pin temperature of 85°C ; with a $R_{thJC} = 0.5\text{ K/W}$ the chip is able to carry $I_D = 174\text{A}$.

²Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical without blown air.

Electrical Characteristics, at $T_j = 25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic Characteristics						
Transconductance	g_{fs}	$V_{DS} \geq 2 \cdot I_D \cdot R_{DS(on)max}$, $I_D = 100A$	88	176	-	S
Input capacitance	C_{iss}	$V_{GS} = 0V$, $V_{DS} = 25V$, $f = 1MHz$	-	6000	7500	pF
Output capacitance	C_{oss}		-	1340	1670	
Reverse transfer capacitance	C_{rss}		-	330	500	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 30V$, $V_{GS} = 4.5V$, $I_D = 100A$, $R_G = 1.3\Omega$	-	18	27	ns
Rise time	t_r		-	25	38	
Turn-off delay time	$t_{d(off)}$		-	98	150	
Fall time	t_f		-	24	36	

Gate Charge Characteristics

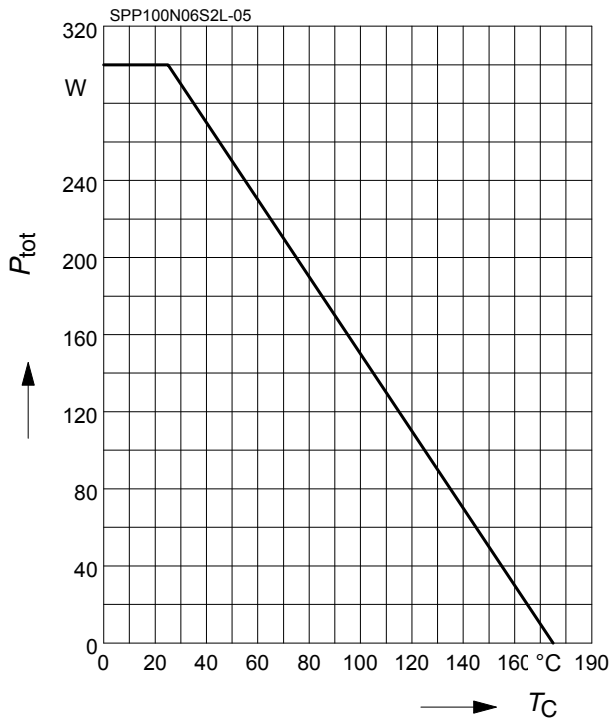
Gate to source charge	Q_{gs}	$V_{DD} = 44\text{V}$, $I_D = 100\text{A}$	-	19	24	nC
Gate to drain charge	Q_{gd}		-	54	80	
Gate charge total	Q_g	$V_{DD} = 44\text{V}$, $I_D = 100\text{A}$, $V_{GS} = 0 \text{ to } 10\text{V}$	-	165	200	
Gate plateau voltage	$V_{(plateau)}$	$V_{DD} = 44\text{V}$, $I_D = 100\text{A}$	-	3.3	-	V

Reverse Diode

Inverse diode continuous forward current	I_S	$T_C = 25^\circ\text{C}$	-	-	100	A
Inverse diode direct current, pulsed	I_{SM}		-	-	400	
Inverse diode forward voltage	V_{SD}	$V_{GS} = 0\text{V}$, $I_F = 80\text{A}$	-	0.9	1.3	V
Reverse recovery time	t_{rr}	$V_R = 30\text{V}$, $I_F = I_S$, $di_F/dt = 100\text{A}/\mu\text{s}$	-	66	80	ns
Reverse recovery charge	Q_{rr}		-	143	180	nC

1 Power dissipation

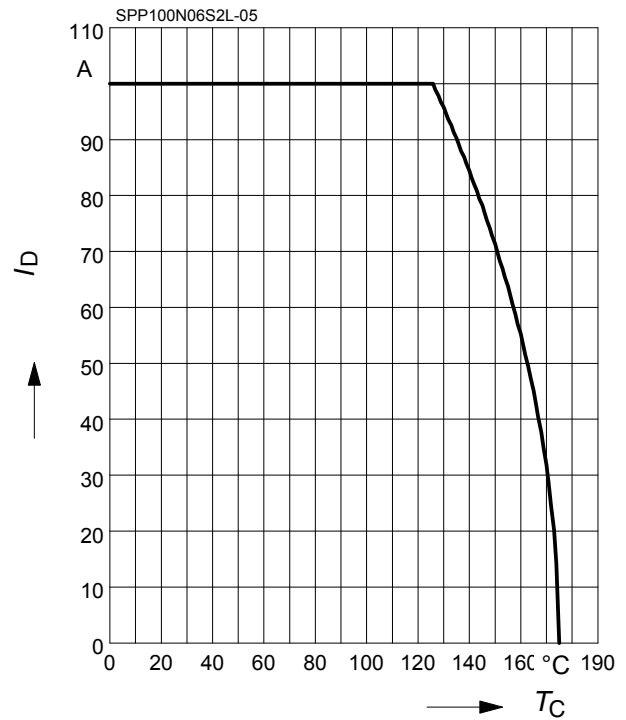
$$P_{\text{tot}} = f(T_C)$$



2 Drain current

$$I_D = f(T_C)$$

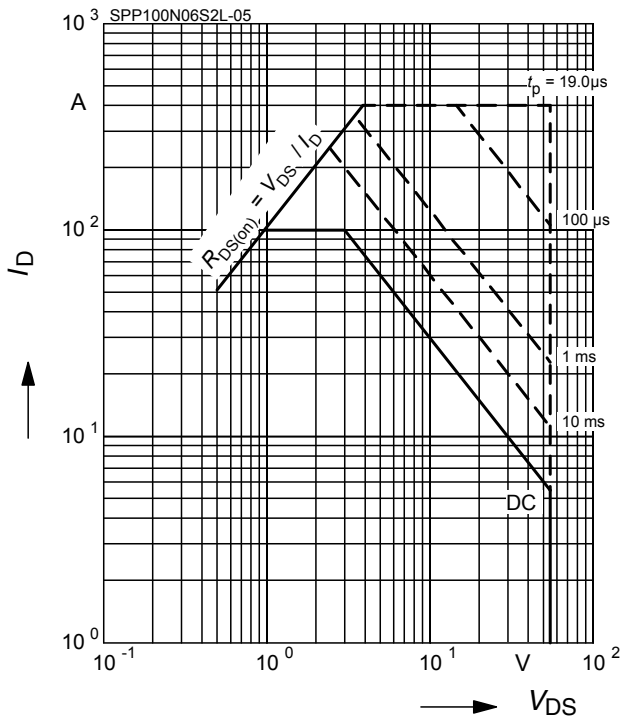
parameter: $V_{GS} \geq 10 \text{ V}$



3 Safe operating area

$$I_D = f(V_{DS})$$

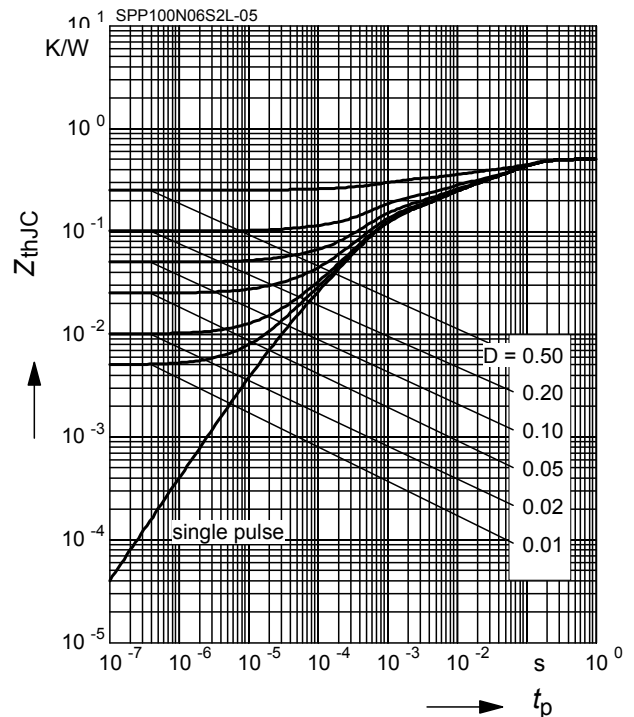
parameter: $D = 0$, $T_C = 25 \text{ °C}$



4 Transient thermal impedance

$$Z_{\text{thJC}} = f(t_p)$$

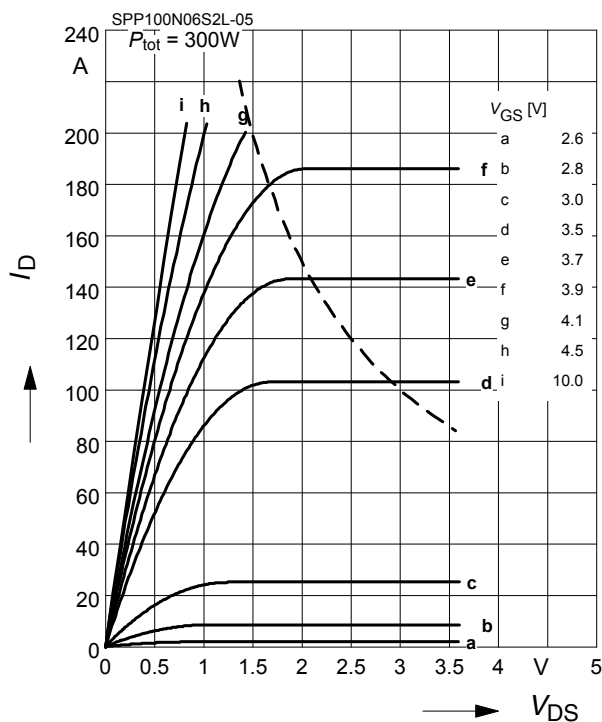
parameter: $D = t_p / T$



5 Typ. output characteristic

$$I_D = f(V_{DS}); T_j = 25^\circ\text{C}$$

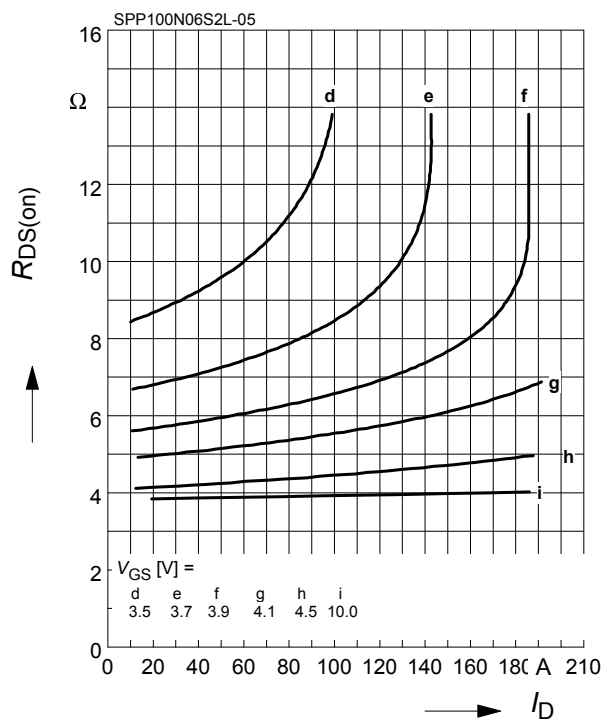
parameter: $t_p = 80 \mu\text{s}$



6 Typ. drain-source on resistance

$$R_{DS(on)} = f(I_D)$$

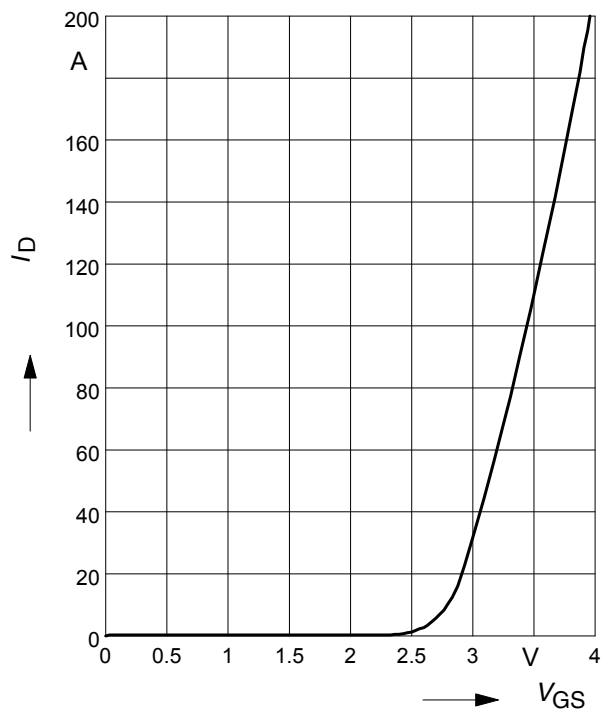
parameter: V_{GS}



7 Typ. transfer characteristics

$$I_D = f(V_{GS}); V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$$

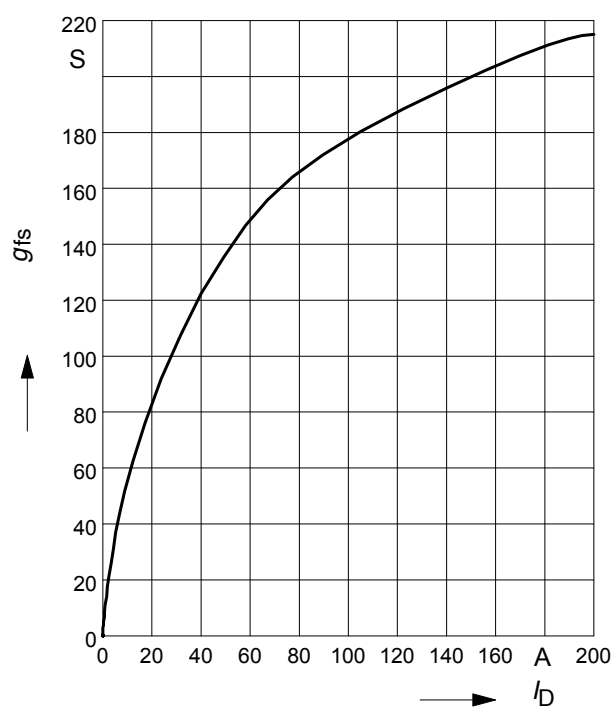
parameter: $t_p = 80 \mu\text{s}$



8 Typ. forward transconductance

$$g_{fs} = f(I_D); T_j = 25^\circ\text{C}$$

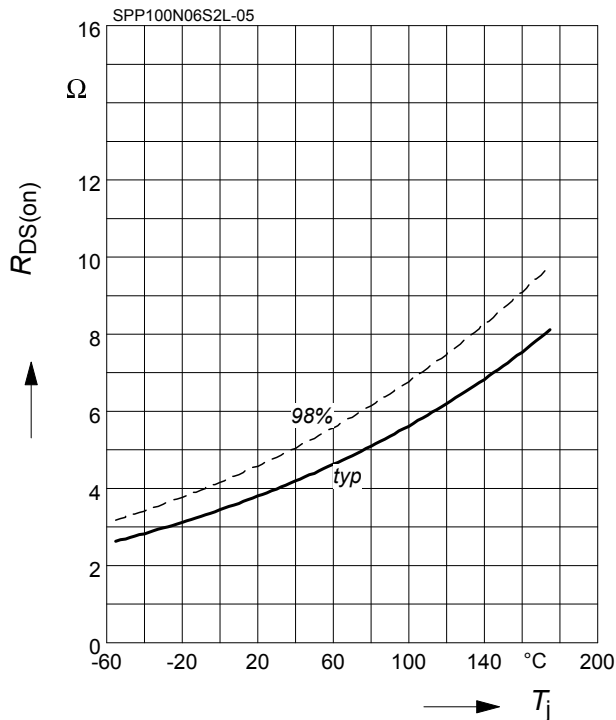
parameter: g_{fs}



9 Drain-source on-state resistance

$$R_{DS(on)} = f(T_j)$$

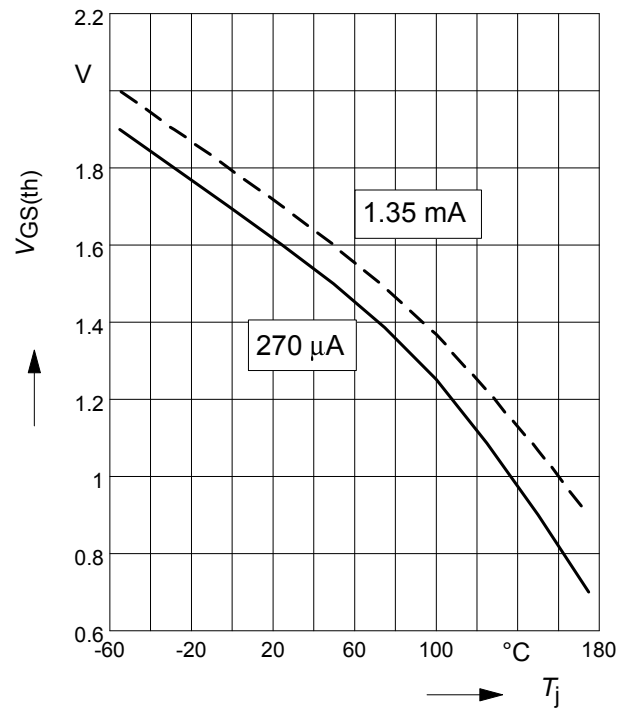
parameter: $I_D = 80 \text{ A}$, $V_{GS} = 10 \text{ V}$



10 Typ. gate threshold voltage

$$V_{GS(th)} = f(T_j)$$

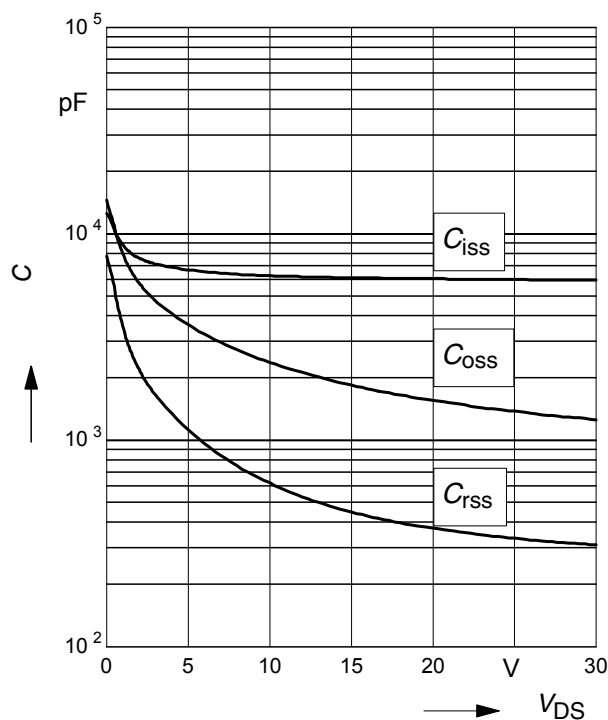
parameter: $V_{GS} = V_{DS}$



11 Typ. capacitances

$$C = f(V_{DS})$$

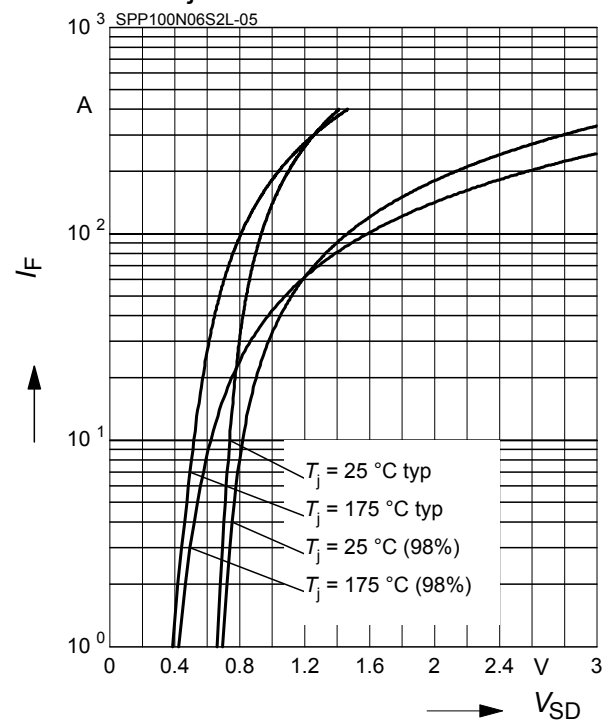
parameter: $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$



12 Forward character. of reverse diode

$$I_F = f(V_{SD})$$

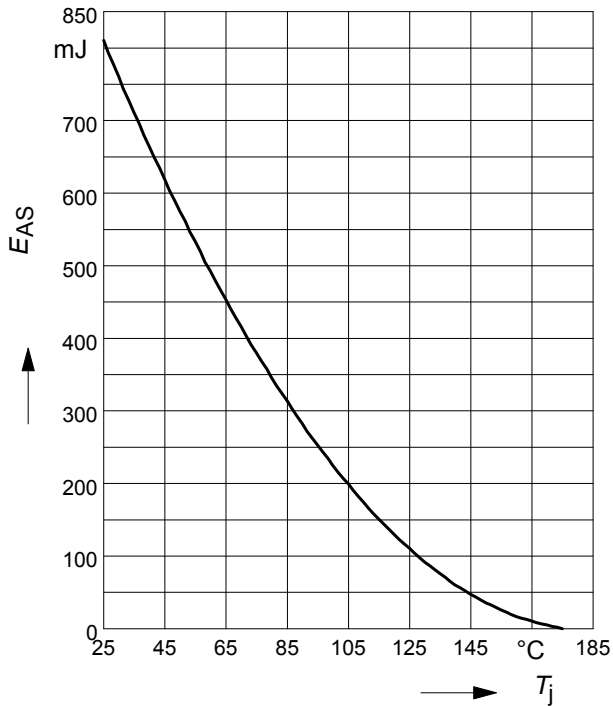
parameter: T_j , $t_p = 80 \mu\text{s}$



13 Typ. avalanche energy

$$E_{AS} = f(T_j)$$

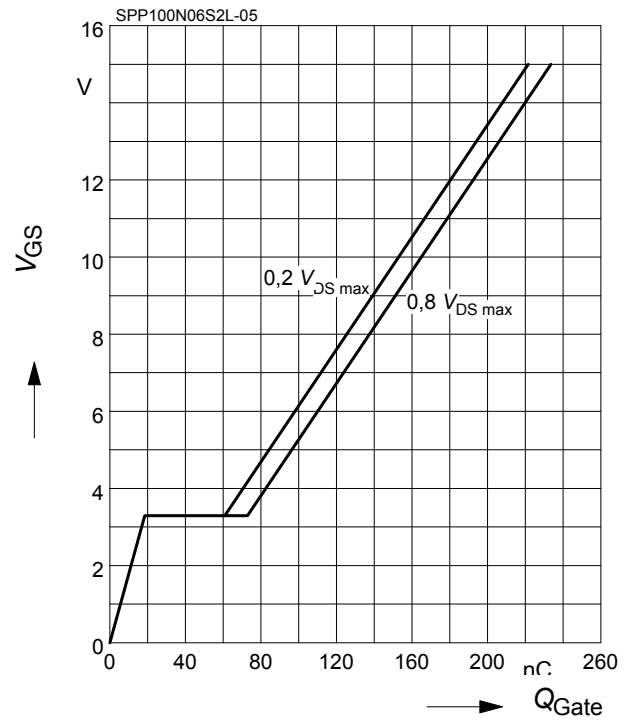
par.: $I_D = 80 \text{ A}$, $V_{DD} = 25 \text{ V}$, $R_{GS} = 25 \Omega$



14 Typ. gate charge

$$V_{GS} = f(Q_{Gate})$$

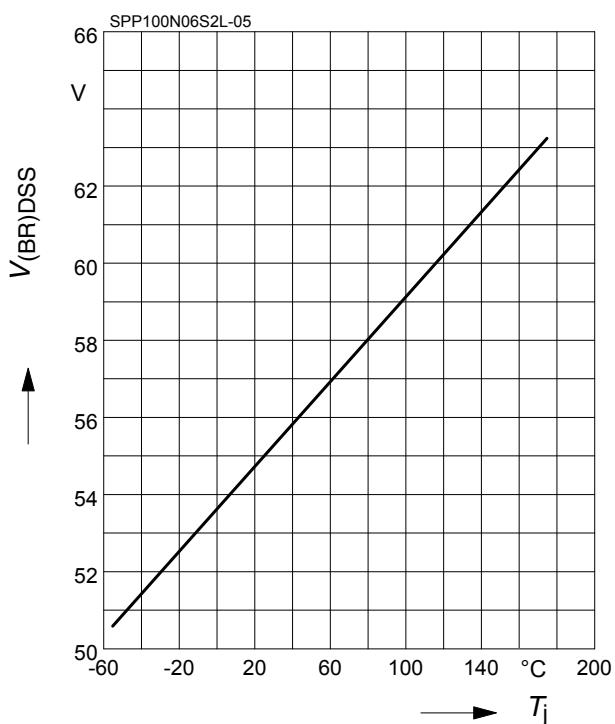
parameter: $I_D = 100 \text{ A}$ pulsed



15 Drain-source breakdown voltage

$$V_{(BR)DSS} = f(T_j)$$

parameter: $I_D = 10 \text{ mA}$



Published by
Infineon Technologies AG,
Bereichs Kommunikation
St.-Martin-Strasse 53,
D-81541 München
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Further information

Please notice that the part number is **BSPP100N06S2L-05** and **BSPB100N06S2L-05**, for simplicity the device is referred to by the term **SPP100N06S2L-05** and **SPB100N06S2L-05** throughout this documentation.