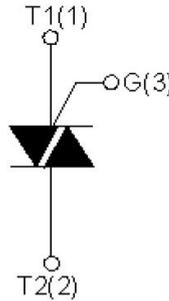
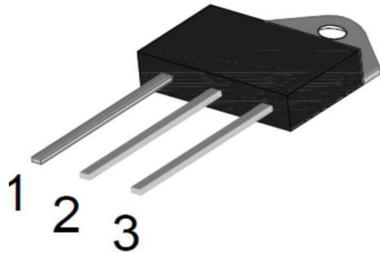


40A TRIACS



BTA41-600/800/1200/1600 TOP3 Plastic Package

BTA41 series triacs, with high ability to withstand the shock loading of large current, provide high dv/dt rate with strong resistance to electromagnetic interference. With high commutation performances, 3 quadrants products especially recommended for use on inductive load.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Storage junction temperature range	T_{stg}	-40 to 150	°C
Operating junction temperature range	T_j	-40 to 125	°C
Repetitive peak off-state voltage ($T_j=25^\circ\text{C}$)	V_{DRM}	600/800/1200/1600	V
Repetitive peak reverse voltage ($T_j=25^\circ\text{C}$)	V_{RRM}	600/800/1200/1600	V
Non repetitive surge peak Off-state voltage	V_{DSM}	$V_{DRM} + 100$	V
Non repetitive peak reverse voltage	V_{RSM}	$V_{RRM} + 100$	V
RMS on-state current ($T_c=80^\circ\text{C}$)	$I_{T(RMS)}$	40	A
Non repetitive surge peak on-state current (full cycle, F=50Hz)	I_{TSM}	400	A
I^2t value for fusing ($t_p=10\text{ms}$)	I^2t	880	A^2s
Critical rate of rise of on-state current ($I_G = 2 \times I_{GT}$)	di/dt	50	$\text{A}/\mu\text{s}$
Peak gate current	I_{GM}	4	A
Average gate power dissipation	$P_{G(AV)}$	1	W
Peak gate power	P_{GM}	10	W

ELECTRICAL CHARACTERISTICS ($T_j=25^\circ\text{C}$ unless otherwise specified)

3 Quadrants

PARAMETER	TEST CONDITIONS	SYMBOL	QUADRANT		VALUES	UNITS
Gate Trigger Current	$V_D = 12\text{V}$ $R_L = 33\Omega$	I_{GT}	I - II - III	MAX	50	mA
Gate Trigger Voltage		V_{GT}	I - II - III	MAX	1.3	V
Off-State Gate Voltage	$V_D = V_{DRM}$ $T_j = 125^\circ\text{C}$ $R_L = 3.3\text{K}\Omega$	V_{GD}	I - II - III	MIN	0.2	V
Latching Current	$I_G = 1.2I_{GT}$	I_L	I - III II	MAX	80 100	mA
Holding Current	$I_T = 100\text{mA}$	I_H		MAX	60	mA
Critical Rate of Rise of Off-State Voltage	$V_D = 2/3V_{DRM}$ Gate Open $T_j = 125^\circ\text{C}$	dV/dt		MIN	1000	V/ μs
	Without snubber $T_j = 125^\circ\text{C}$	$(dV/dt)_c$		MIN	20	V/ μs

4 Quadrants

PARAMETER	TEST CONDITIONS	SYMBOL	QUADRANT		VALUES	UNITS
Gate Trigger Current	$V_D = 12\text{V}$ $R_L = 33\Omega$	I_{GT}	I - II - III	MAX	50	mA
			IV		70	
Gate Trigger Voltage		V_{GT}	ALL	MAX	1.5	V
Off-State Gate Voltage	$V_D = V_{DRM}$ $T_j = 125^\circ\text{C}$ $R_L = 3.3\text{K}\Omega$	V_{GD}	ALL	MIN	0.2	V
Latching Current	$I_G = 1.2I_{GT}$	I_L	I - III - IV II	MAX	90 100	mA
Holding Current	$I_T = 100\text{mA}$	I_H		MAX	80	mA
Critical Rate of Rise of Off-State Voltage	$V_D = 2/3V_{DRM}$ Gate Open $T_j = 125^\circ\text{C}$	dV/dt		MIN	500	V/ μs
	Without snubber $T_j = 125^\circ\text{C}$	$(dV/dt)_c$		MIN	30	V/ μs

STATIC CHARACTERISTICS

PARAMETER	TEST CONDITIONS	SYMBOL	VALUE (MAX)	UNITS
On-State Voltage	$I_{TM} = 60\text{A}$ $t_p = 380\mu\text{s}$	$T_j = 25^\circ\text{C}$ V_{TM}	1.55	V
Off-State Leakage Current	$V_D = V_{DRM}$ $V_R = V_{RRM}$	$T_j = 25^\circ\text{C}$ I_{DRM}	10	μA
		$T_j = 125^\circ\text{C}$ I_{RRM}	5	mA

THERMAL RESISTANCES

PARAMETER	SYMBOL	VALUE (MAX)	UNITS
junction to case(AC)	$R_{th(j-c)}$	0.9	$^\circ\text{C/W}$

ORDERING INFORMATION

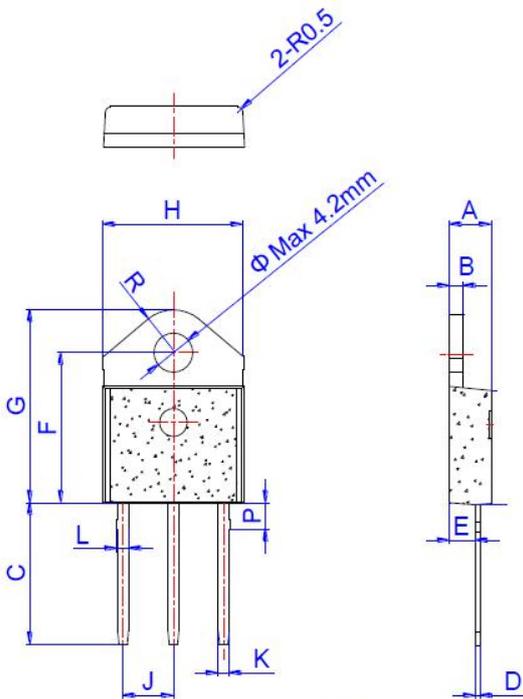
BTA 41 - 600 BW

(a) (b)

(a) = 600: VDRM/VRRM \geq 600
 = 800: VDRM/VRRM \geq 800
 = 1200: VDRM/VRRM \geq 1200
 = 1600: VDRM/VRRM \geq 1600

(b) = BW: $I_{GT3} \leq 50\text{mA}$
 = B: $I_{GT1-3} \leq 50\text{mA}$ $I_{GT4} \leq 70\text{mA}$

TOP3 PACKAGE OUTLINE AND DIMENSION



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	4.40		4.60	0.173		0.181
B	1.45		1.55	0.057		0.061
C	14.35		15.60	0.565		0.614
D	0.50		0.70	0.020		0.028
E	2.70		2.90	0.106		0.114
F	15.80		16.50	0.622		0.650
G	20.40		21.10	0.803		0.831
H	15.10		15.50	0.594		0.610
J	5.40		5.65	0.213		0.222
K	1.10		1.40	0.043		0.055
L	1.35		1.50	0.053		0.059
P	2.80		3.00	0.110		0.118
R		4.35			0.171	

CHARACTERISTIC CURVES

FIG.1 Maximum power dissipation versus RMS on-state current

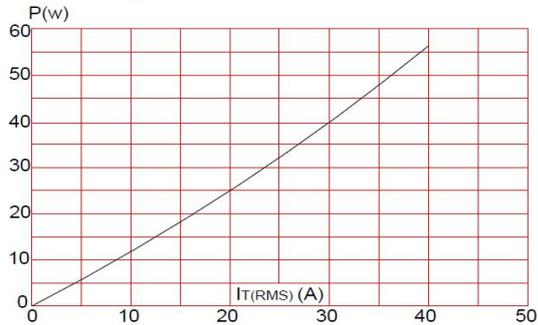


FIG.3: Surge peak on-state current versus number of cycles

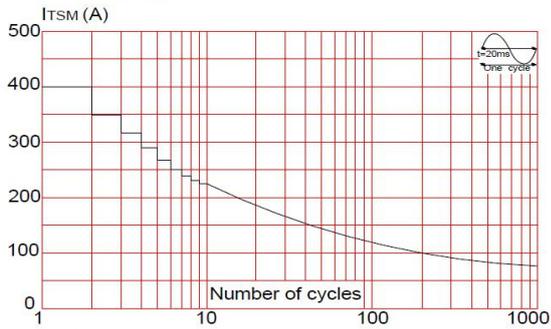


FIG.5: Non-repetitive surge peak on-state current for a sinusoidal pulse with width $t_p < 20\text{ms}$, and corresponding value of I^2t ($di/dt < 50\text{A}/\mu\text{s}$)

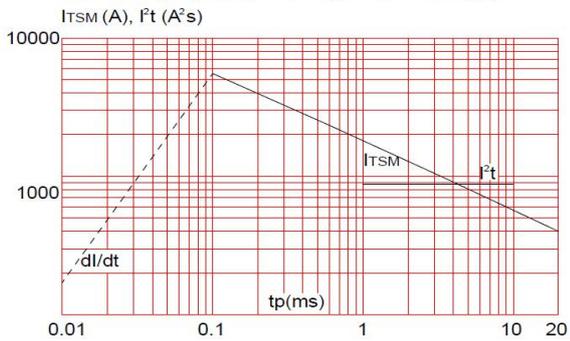


FIG.2: RMS on-state current versus case temperature

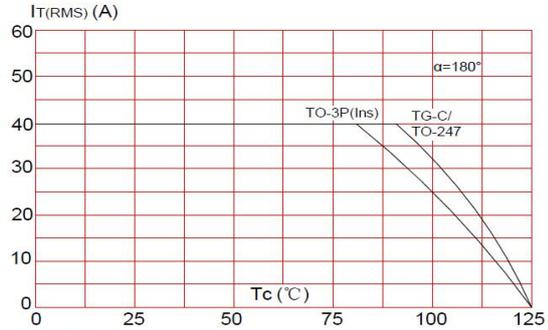


FIG.4: On-state characteristics (maximum values)

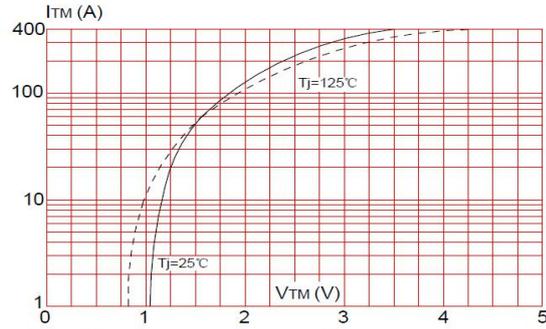
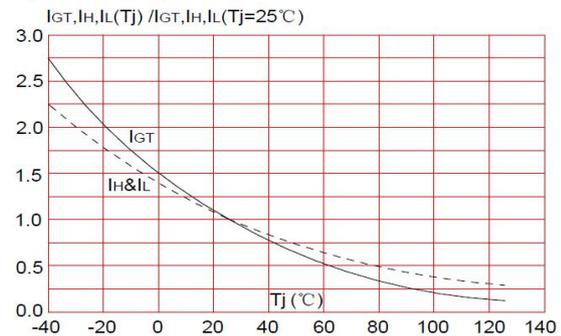


FIG.6: Relative variations of gate trigger current, holding current and latching current versus junction temperature





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Customer Notes

Component Disposal Instructions

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

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Continental Device India Pvt. Limited
C-120 Naraina Industrial Area, New Delhi 110 028, India.
Telephone + 91-11-2579 6150, 4141 1112 Fax + 91-11-2579 5290, 4141 1119
email@cdil.com www.cdil.com
CIN No. U32109DL1964PLC004291