FUJITSU

UV ERASABLE 65536-BIT READ ONLY MEMORY

MBM 2764-20
MBM 2764-25
MBM 2764-30

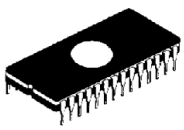
January 1984
Edition 4.0

MOS 8192x8BIT UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

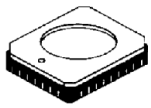
The Fujitsu MBM 2764 is a high speed 65,536-bit static N-channel MOS erasable and electrically reprogrammable read only memory (EPROM). It is especially well suited for applications where rapid turn-around and/or bit pattern experimentation are important.

A 28-pin Dual-In-Line package and a 32-pad Leadless-Chip-Carrier with a transparent lid are used to package the MBM 2764. The transparent lid allows the user to expose the device to ultraviolet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can then be written into the memory.

The MBM 2764 is fabricated using N-MOS double polysilicon gate technology with single transistor stacked gate cells. It is organized as 8192 words by 8 bits for use in microprocessor applications. Single +5V operation greatly facilitates its use in systems.



CERAMIC PACKAGE
DIP-28C-C01

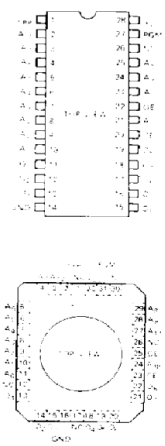


CERAMIC PACKAGE
LCC-32C-A01

- 8192 words x 8 bits organization, fully decoded
- Simple programming requirements
- Single location programming
- Programmable utilizing the Quick Pro™ Algorithm
- Programs with one 50ms or 1ms pulse
- Low power requirement
  - Active : 788mW (550mW)
  - Standby : 184mW (193mW)

  (Value in parentheses is for "AB" version.)
- No clocks required (fully static operation)
- TTL compatible inputs/outputs
- Three-state output with OR-tie capability
- Output Enable ($\overline{OE}$) pin for simplified memory expansion
- Fast access time:
  - 200ns max. (MBM 2764-20)
  - 250ns max. (MBM 2764-25)
  - 300ns max. (MBM 2764-30)
- Single +5V operation
- Standard 28-pin DIP package and 32-pad LCC
- Interchangeable with Intel 2764

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Temperature under Bias	T_{BIAS}	-25 to +85	°C
Storage Temperature	T_{STG}	-65 to +125	°C
All Inputs/Outputs Voltage with Respect to GND	V_{IN}, V_{OUT}	-0.6 to +7	V
V_{PP} Voltage with Respect to GND	V_{PP}	-0.6 to +22	V
Supply Voltage with Respect to GND	V_{CC}	-0.6 to +7	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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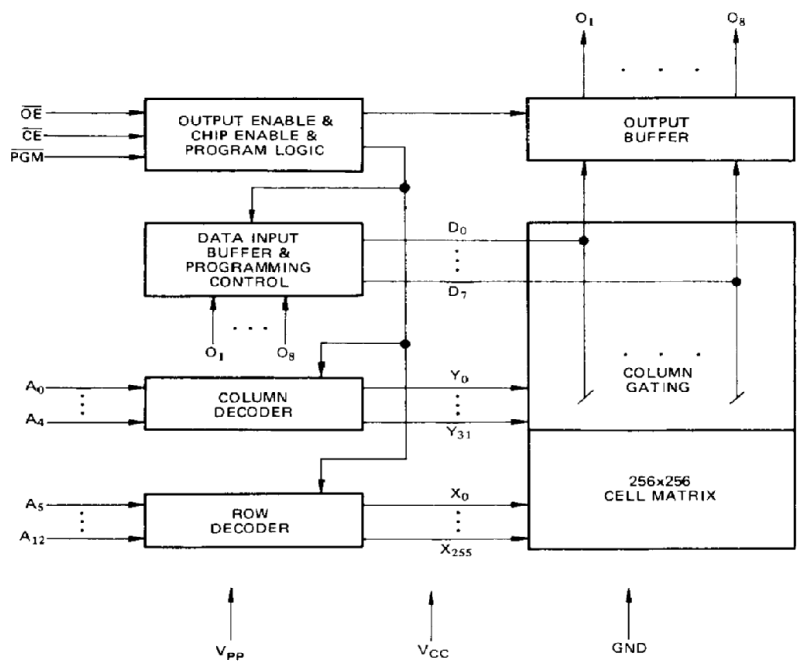
Fig. 1 — MBM 2764 BLOCK DIAGRAM



CAPACITANCE (T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance (V_{IN} = 0V)	C_{IN}	—	4	6	pF
Output Capacitance (V_{OUT} = 0V)	C_{OUT}	—	8	12	pF

FUNCTIONS AND PIN CONNECTIONS

Function (Pin No.) / Mode	Address Input (2~10, 23~25, 21)	Data I/O (11~13, 15~19)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{CC} (28)	V_{PP} (1)	GND (14)
Read	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	GND
Output Disable	Don't Care	High-Z	V_{IL}	V_{IH}	Don't Care	V_{CC}	V_{CC}	GND
				Don't Care	V_{IL}			
Standby	Don't Care	High-Z	V_{IH}	Don't Care	Don't Care	V_{CC}	V_{CC}	GND
Program	A_{IN}	D_{IN}	V_{IL}	V_{IH}	V_{IL}	V_{CC}	V_{PP}	GND
Program Verify	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{PP}	GND
Program Inhibit	Don't Care	High-Z	V_{IH}	Don't Care	Don't Care	V_{CC}	V_{PP}	GND

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RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
V_{CC} Supply Voltage*1	V_{CC}	4.75 (4.5)*2	5.0	5.25 (5.5)*2	V
V_{PP} Supply Voltage	V_{PP}	V_{CC} −0.6	–	V_{CC} + 0.6	V
Input High Voltage	V_{IH}	2.0	–	V_{CC} + 1	V
Input Low Voltage	V_{IL}	−0.1	–	0.8	V
Operating Temperature	T_A	0		70	°C

Note: *1 V_{CC} must be applied either before or coincident with V_{PP} and removed either after or coincident with V_{PP}.
*2 Value in parentheses is for "AB" version.

DC CHARACTERISTICS

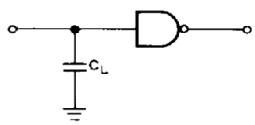
(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit
Input Load Current (V_{IN} = 5.25V)*1	I_{LI}			10	μA
Output Leakage Current (V_{OUT} = 5.25V)*1	I_{LO}			10	μA
V_{CC} Standby Current ($\overline{CE}$ = V_{IH})	I_{CC1}			35	mA
V_{CC} Supply Current ($\overline{CE}$ = V_{IL})	I_{CC2}			150 (100)*2	mA
V_{PP} Supply Current (V_{PP} = V_{CC} ± 0.6V)	I_{PP}			15	mA
Output Low Voltage (I_{OL} = 2.1mA)	V_{OL}			0.45	V
Output High Voltage (I_{OH} = −400μA)	V_{OH}	2.4			V

Note: *1 V_{IN} and V_{OUT} voltage for "AB" parts is 5.5V.
*2 Value in parentheses is for "AB" version.

Fig. 2 – AC TEST CONDITIONS (INCLUDING PROGRAMMING)

Input Pulse Levels:	0.8V to 2.2V
Input Rise and Fall Times:	≤ 20ns
Timing Measurement Reference Levels:	1.0V and 2.0V for inputs 0.8V and 2.0V for outputs
Output Load:	1 TTL gate and C_L = 100pF



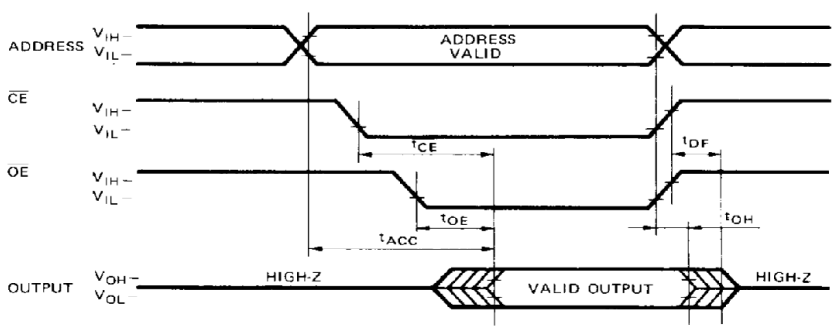
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	MBM 2764-20			MBM 2764-25			MBM 2764-30			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Address Access Time*1	t_{ACC}			200			250			300	ns
$\overline{CE}$ to Output Delay	t_{CE}			200			250			300	ns
$\overline{OE}$ to Output Delay*1	t_{OE}	10		70	10		100	10		120	ns
Address to Output Hold	t_{OH}	0			0			0			ns
Output Enable High to Output Float*2	t_{DF}	0		60	0		60	0		105	ns

Notes: *1 $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
*2 t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
Output Float is defined as the point where data is no longer driven.

OPERATION TIMING DIAGRAM



CHARACTERISTICS CURVES

Fig. 3 –SUPPLY CURRENT (STANDBY) vs SUPPLY VOLTAGE

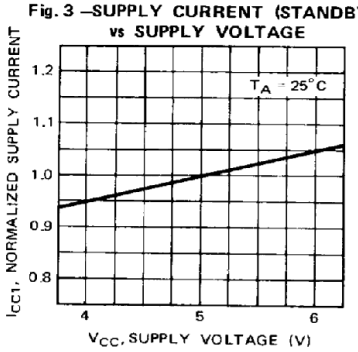


Fig. 4 – SUPPLY CURRENT (STANDBY) vs AMBIENT TEMPERATURE

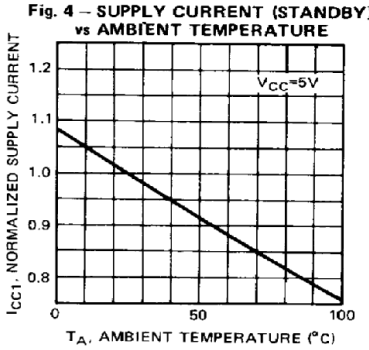


Fig. 5 – SUPPLY CURRENT (ACTIVE) vs SUPPLY VOLTAGE

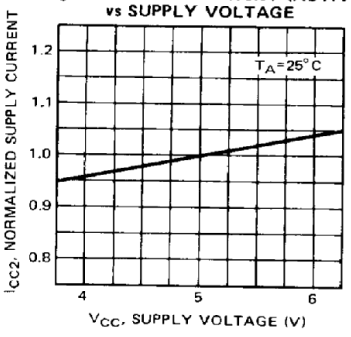


Fig. 6 – SUPPLY CURRENT (ACTIVE) vs AMBIENT TEMPERATURE

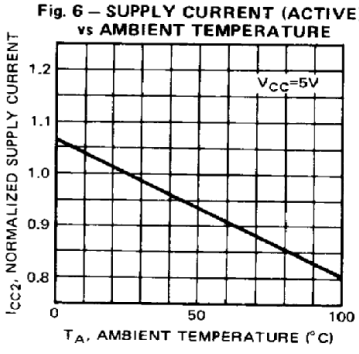


Fig. 7 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

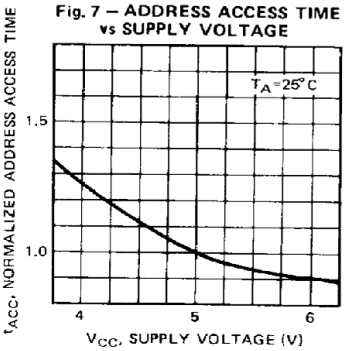
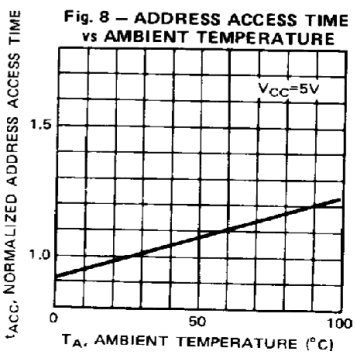


Fig. 8 – ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE



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CHARACTERISTICS CURVES (continued)

Fig. 9 – $\overline{CE}$ TO OUTPUT DELAY vs AMBIENT TEMPERATURE

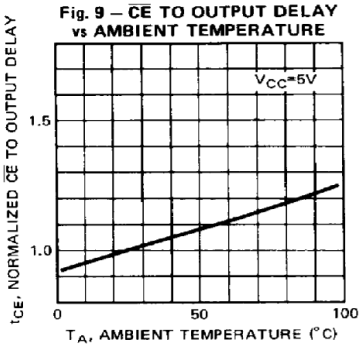


Fig. 10 – $\overline{OE}$ TO OUTPUT DELAY vs AMBIENT TEMPERATURE

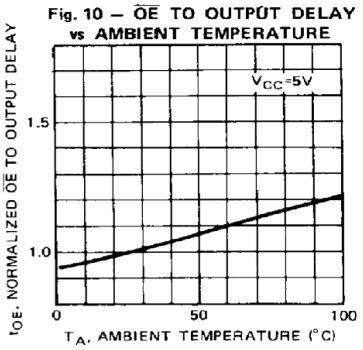


Fig. 11 – $\overline{OE}$ HIGH TO OUTPUT FLOAT vs AMBIENT TEMPERATURE

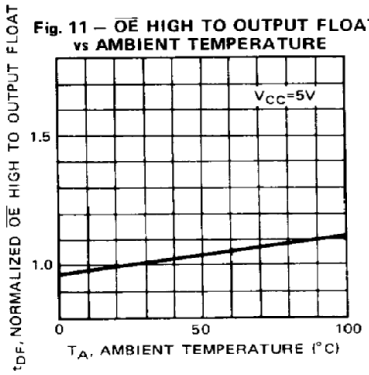


Fig. 12 – OUTPUT SOURCE CURRENT vs OUTPUT HIGH VOLTAGE

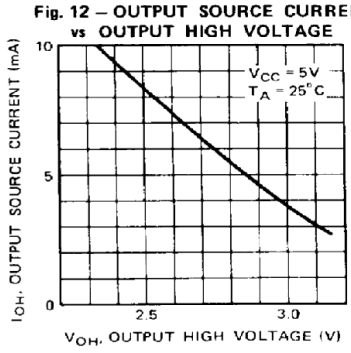


Fig. 13–OUTPUT SINK CURRENT vs OUTPUT LOW VOLTAGE

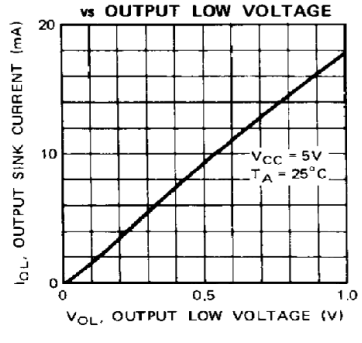
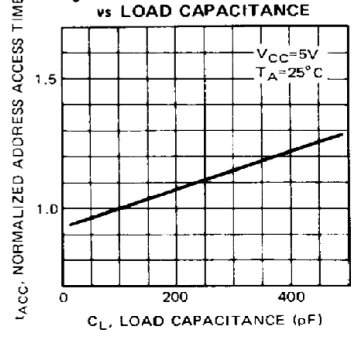


Fig. 14 – ADDRESS ACCESS TIME vs LOAD CAPACITANCE



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PROGRAMMING/ERASING INFORMATION

MEMORY CELL DESCRIPTION

The MBM 2764 is fabricated using a single-transistor stacked gate cell construction, implemented via double-layer polysilicon technology. The individual cells consist of a bottom floating gate and a top select gate (see Fig. 15). The top gate is connected to the row decorder, while the floating gate is used for charge storage. The cell is programmed by the injection of high energy electrons through the oxide and onto the floating gate. The presence of the charge on the floating gate causes a shift in the cell threshold (refer to Fig. 16). In the initial state, the cell has a low threshold (V_{TH1}) which will enable the transistor to be turned on when the cell is selected (via the top select gate). Programming shifts the threshold to a higher level (V_{TH0}), thus preventing the cell transistor from turning on when selected. The status of the cell (i.e., whether programmed or not) can be determined by examining its state at the sense threshold (V_{THS}), as indicated by the dotted line in Fig. 16.

Fig. 15 – MEMORY CELL

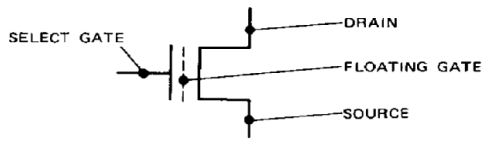
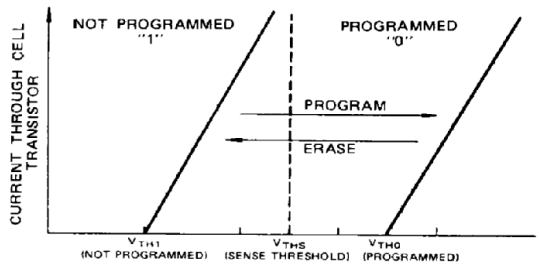


Fig. 16 – MEMORY CELL THRESHOLD SHIFT



PROGRAMMING

Upon delivery from Fujitsu, or after each erasure (see Erasure section), the MBM 2764 has all 65,536 bits in the "1", or high, state. "0's" are loaded into the MBM 2764 through the procedure of programming.

Normal Programming

The programming mode is entered when +21V is applied to the V_{PP} pin and $\overline{CE}$ and $\overline{PGM}$ are both at V_{IL}. During programming, $\overline{CE}$ is kept at V_{IL}. A 0.1μF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. 8 bit patterns are placed on the respective data output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a 50 msec, TTL low-level pulse is applied to the $\overline{PGM}$ input to accomplish the programming. The procedure can be done manually, address by address, randomly, or automatically via the proper circuitry. All that is required is that one 50 msec program pulse be applied at each address to be programmed. It is necessary that this program pulse width not exceed 55 msec. Therefore, applying a DC level to the $\overline{PGM}$ input is prohibited when programming.

Quick Programming

In addition to the standard 50 msec pulse width programming procedure, the MBM 2764 can be programmed with a fast programming algorithm designed by Fujitsu called Quick Pro™. The algorithm (shown Fig. 17) untilizes a sequence of ONE millisecond pulse to program each location.
The programming mode is entered when +21V and +6V are applied to the V_{PP} pin and V_{CC} pin respectively, and $\overline{PGM}$ and $\overline{OE}$ are V_{IH}. During programming, $\overline{CE}$ is kept at V_{IL}. A 0.1μF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients which could damage the device. The address to be programmed is applied to the proper address pins. The 8 bit pattern are placed on the respective data output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a 1 msec, TTL low-level pulse is applied to the $\overline{PGM}$ pin and after that additional pulse is applied to the $\overline{PGM}$ pin to accomplish the programming.

Procedure of Quick Pro™ (Refer to Fig. 17.)

1) Input the start address (Address=G)
2) Set the V_{CC} = 6V and V_{PP} = 21V

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PROGRAMMING/ERASING INFORMATION (continued)

3) Data input.
4) Compare the input data. If data are FF, jump to the 11). If data are not FF, proceed the next step.
5) Set the number of programming pulse to 0. (X=0)
6) Apply ONE programming pulse to $\overline{PGM}$ pin (t_{PW} =1 ms Typ.).
7) Count the programming pulse (X=X+1)
8) Compare the number of programming pulse. If X=20, jump to the 10). If X<20, proceed the next step.
9) Verify the data. If programmed data are the same as input data, proceed the next step. If programming data are not the same as input data, repeat the 6) thru 8).
10) Apply the additional programming pulse to the $\overline{PGM}$ pin (1 ms x X or X ms x 1).
11) Compare the address. If the programmed address is end address, proceed the next step.
If the programmed address is not end address, proceed from step 3) for next address (G+1).
12) Verify the data. If programmed data are not the same as input data, the part is no good. If programmed data are the same as input data, programming is end.

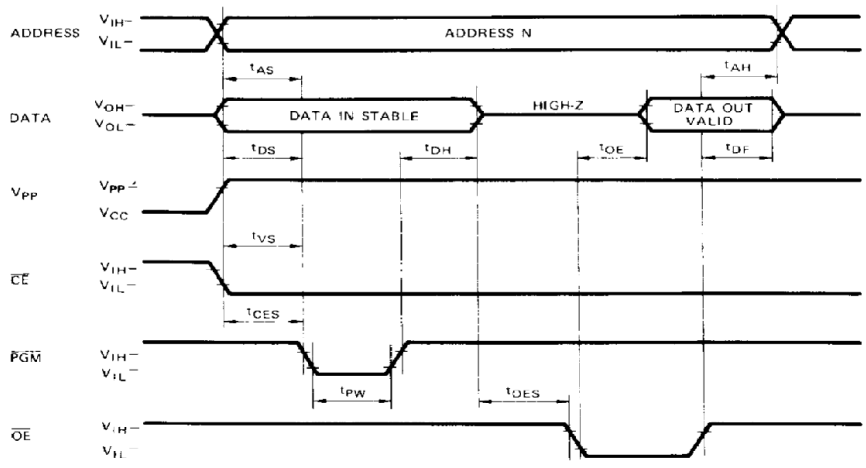
All that is required is that one 1 msec program pulse be applied at each address to be programmed. It is necessary that one program pulse width does not exceed 1.05 msec. Therefore, applying a DC level to the $\overline{PGM}$ input is prohibited when programming.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the MBM 2764 to an ultraviolet light source. A dosage of 15 W-seconds/cm^2 is required to completely erase an MBM 2764. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (Å)) with intensity of 12000μW/cm^2 for 15 to 20 minutes. The MBM 2764 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the MBM 2764 and similar devices, will erase with light sources having wavelengths shorter than 4000Å. Although erasure time will be much longer than with UV source at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the MBM 2764, and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

PROGRAMMING WAVEFORM



1. Normal Programming

DC CHARACTERISTICS

(T_A = 25±5°C, V_{CC}*1 = 5V±5%, V_{PP}*2 = 21±0.5V)

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IN} = 5.25V/0.45V)	I_{LI}			10	μA
V_{PP} Supply Current During Programming Pulse ($\overline{CE}$ = $\overline{PGM}$ = V_{IL})	I_{PP}			30	mA
V_{CC} Supply Current	I_{CC}			150 (100) *3	mA
Input Low Level	V_{IL}	-0.1		0.8	V
Input High Level	V_{IH}	2.0		V_{CC}+1	V
Output Low Voltage During Verify (I_{OL} = 2.1mA)	V_{OL}			0.45	V
Output High Voltage During Verify (I_{OH} = -400μA)	V_{OH}	2.4			V

Note: *1 V_{CC} must be applied either coincidently or before V_{PP} and removed either coincidently or after V_{PP}.
*2 V_{PP} must not be greater than 22 volts including overshoot. Permanent device damage may occur if the device is taken out or put into socket remaining V_{PP} = 21 volts. Also, during $\overline{CE}$=$\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from V_{CC} to 21 volts or vise-versa.
*3 Value in parentheses is for "AB" version.

AC CHARACTERISTICS

(T_A = 25±5°C, V_{CC} = 5V±5%, V_{PP} = 21±0.5V)

Parameter	Symbol	Min	Typ	Max	Unit
Address Setup Time	t_{AS}	2			μs
Chip Enable Setup Time	t_{CES}	2			μs
Output Enable	t_{OES}	2			μs
Data Setup Time	t_{DS}	2			μs
Address Hold Time	t_{AH}	0			μs
Data Hold Time	t_{DH}	2			μs
Output Enable to Output Float Delay	t_{DF}	0		130	ns
Data Valid from Output Enable	t_{OE}			150	ns
V_{PP} Setup Time	t_{VS}	2			μs
$\overline{PGM}$ Pulse Width	t_{PW}	45	50	55	ms

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PROGRAMMING/ERASING INFORMATION (continued)

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2. Quick Programming

DC CHARACTERISTICS

(T_A = 25±5°C, V_{CC}*1 = 6V±0.25V, V_{PP}*2 = 21V±0.5V

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IN} = 6.25V/0.45V)	I_{LI}			10	μA
V_{PP} Supply Current During Programming Pulse ($\overline{CE}$ = $\overline{PGM}$ = V_{IL})	I_{PP}			30	mA
V_{CC} Supply Current	I_{CC}			150 (100)*3	mA
Input Low Level	V_{IL}	-0.1		0.8	V
Input High Level	V_{IH}	2.0		V_{CC}+1	V
Output Low Voltage During Verfify (I_{OL} = 2.1mA)	V_{OL}			0.45	V
Output High Voltage During Verify (I_{OH} = -400μA)	V_{OH}	2.4			V

Note: *1 V_{CC} must be applied either coincidently or before V_{PP} and removed either concidently or after V_{PP}.
*2 V_{PP} must not be greater than 22 volts including overshoot. Permanent device damage may occuring the device is taken out or put into socket remaining V_{PP} = 21 volts. Also, during $\overline{CE}$ = $\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from V_{IL} to V_{PP} volts or vise-versa.
*3 Value in parentheses is for "AB" version.

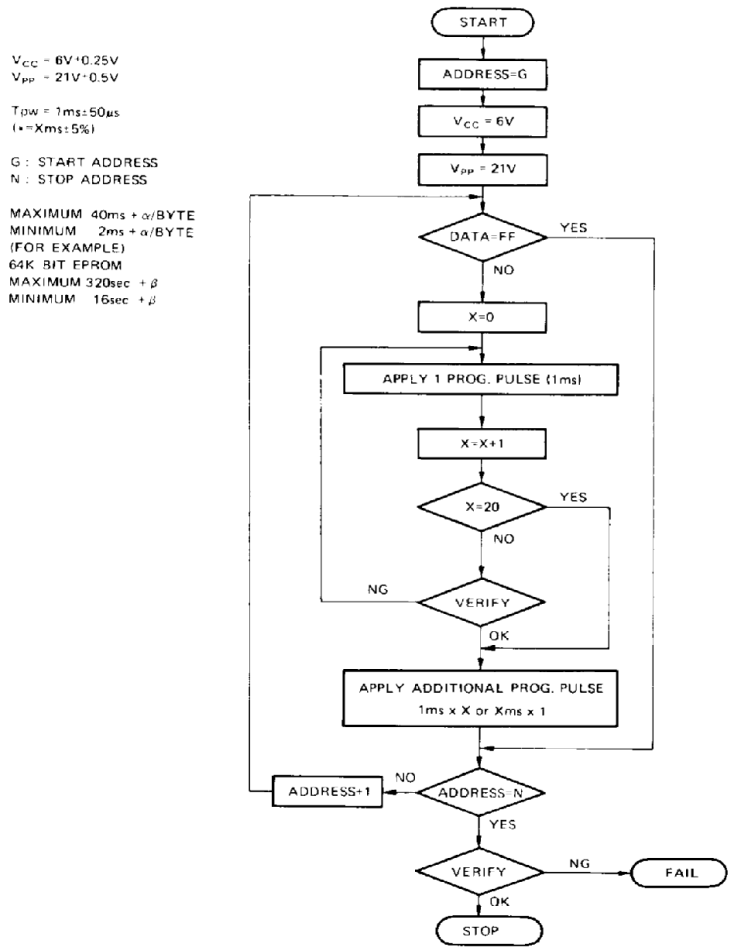
AC CHARACTERISTICS

(T_A = 25±5°C, V_{CC} = 6V±0.25V, V_{PP} = 21V±0.5V)

Parameter	Symbol	Min	Typ	Max	Unit
Address Setup Time	t_{AS}	2			μs
Chip Enable Setup Time	t_{CES}	2			μs
Output Enable Setup Time	t_{OES}*	2			μs
Data Setup Time	t_{DS}	2			μs
Address Hold Time	t_{AH}	0			μs
Data Hold Time	t_{DH}*	2			μs
Output Enable to Output Float Delay	t_{DF}	0		130	ns
Data Valid from Output Enable	t_{OE}			150	ns
V_{PP} Setup Time	t_{VS}	2			μs
$\overline{PGM}$ Pulse Width	t_{PW}	0.95	1	1.05	ms

* $t_{DH} + t_{OES} \geq 50\mu s$

Fig. 17—PROGRAMMING FLOW CHART FOR Quick Pro™



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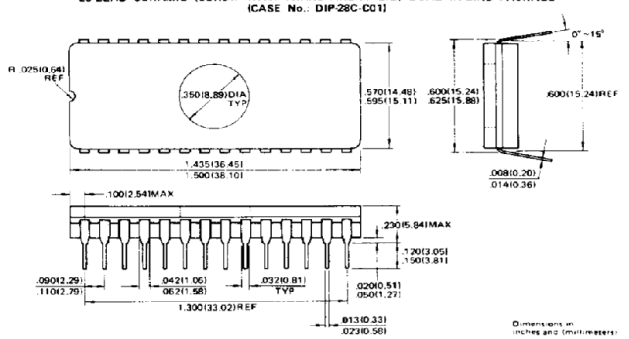
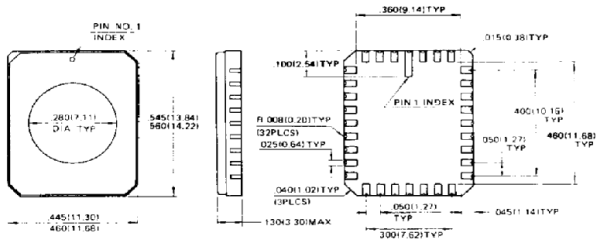
PACKAGE DIMENSIONS

28-LEAD CERAMIC (CERDIP WITH TRANSPARENT LID) DUAL IN-LINE PACKAGE
(CASE No.: DIP-28C-C01)



Dimensions in inches and (millimeters)

32-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No. : LCC-32C-A01)



Dimensions in inches (millimeters)

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