MOTOROLA

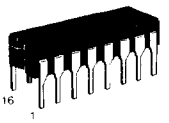
MC14501UB

TRIPLE GATE

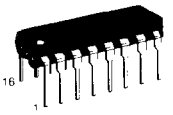
DUAL 4-INPUT "NAND" GATE
2-INPUT "NOR/OR" GATE
8-INPUT "AND/NAND" GATE

The MC14501UB is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired. Additional characteristics can be found on the Family Data Sheet.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Logic Swing Independent of Fanout
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648

D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

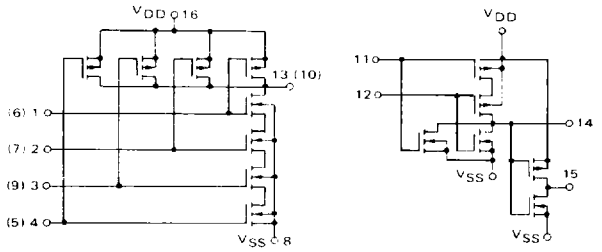
T_A = -55° to 125°C for all packages.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	-0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

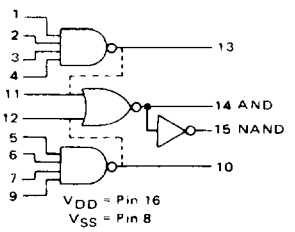
*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P and D/DW" Packages: 7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

CIRCUIT SCHEMATIC



Numbers in parenthesis are for second 4 input gate

LOGIC DIAGRAM
(POSITIVE LOGIC)



Use Dotted Connection Externally to Obtain 8-Input AND/NAND

Note: Pin 14 must not be used as an input to the inverter.

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ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	−55°C Min	−55°C Max	25°C Min	25°C Typ #	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage "0" Level (V_O = 3.6 or 1.4 Vdc)	V_{IL}	5.0	—	1.5	—	2.25	1.5	—	1.4	Vdc
(V_O = 7.2 or 2.8 Vdc)		10	—	3.0	—	4.50	3.0	—	2.9	
(V_O = 11.5 or 3.5 Vdc)		15	—	3.75	—	6.75	3.75	—	3.6	
(V_O = 1.4 or 3.6 Vdc) "1" Level	V_{IH}	5.0	3.6	—	3.5	2.75	—	3.5	—	Vdc
(V_O = 2.8 or 7.2 Vdc)		10	7.1	—	7.0	5.50	—	7.0	—	
(V_O = 3.5 or 11.5 Vdc)		15	11.4	—	11.25	8.25	—	11	—	
Output Drive Current	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−1.2	—	−1.0	−1.7	—	−0.7	—	
(V_{OH} = 4.6 Vdc)		5.0	−0.25	—	−0.2	−0.36	—	−0.14	—	
(V_{OH} = 9.5 Vdc) NAND*		10	−0.62	—	−0.5	−0.9	—	−0.35	—	
(V_{OH} = 13.5 Vdc)		15	−1.8	—	−1.5	−3.5	—	−1.1	—	
(V_{OH} = 2.5 Vdc) NOR		5.0	−2.1	—	−1.75	−3.0	—	−1.22	—	mAdc
(V_{OH} = 4.6 Vdc)		5.0	−0.42	—	−0.35	−0.63	—	−0.24	—	
(V_{OH} = 9.5 Vdc		10	−1.06	—	−0.88	−1.58	—	−0.62	—	
(V_{OH} = 13.5 Vdc)		15	−3.1	—	−2.63	−6.12	—	−1.84	—	
(V_{OH} = 2.5 Vdc) NOR-		5.0	−3.6	—	−3.0	−5.1	—	−2.1	—	mAdc
(V_{OH} = 4.6 Vdc)		5.0	−0.72	—	−0.6	−1.08	—	−0.42	—	
(V_{OH} = 9.5 Vdc) Inverter		10	−1.8	—	−1.5	−2.7	—	−1.05	—	
(V_{OH} = 13.5 Vdc)		15	−5.4	—	−4.5	−10.5	—	−3.15	—	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
(V_{OL} = 0.5 Vdc) NAND*		10	1.6	—	1.3	2.25	—	0.9	—	
(V_{OL} = 1.5 Vdc)		15	4.2	—	3.4	8.8	—	2.4	—	
(V_{OL} = 0.4 Vdc) NOR		5.0	0.92	—	0.77	1.32	—	0.54	—	mAdc
(V_{OL} = 0.5 Vdc)		10	2.34	—	1.95	3.37	—	1.36	—	
(V_{OL} = 1.5 Vdc)		15	6.12	—	5.1	13.2	—	3.57	—	
(V_{OL} = 0.4 Vdc) NOR-		5.0	1.54	—	1.28	2.2	—	0.90	—	mAdc
(V_{OL} = 0.5 Vdc) Inverter		10	3.90	—	3.25	5.63	—	2.27	—	
(V_{OL} = 1.5 Vdc)		15	10.2	—	8.5	22	—	5.95	—	
Input Current	I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0	—	0.25	—	0.0005	0.25	—	7.5	μAdc
		10	—	0.5	—	0.0010	0.5	—	15	
		15	—	1.0	—	0.0015	1.0	—	30	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.2 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (2.4 μA/kHz) f + I_{DD}							
		15	I_T = (3.6 μA/kHz) f + I_{DD}							

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.004.

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SWITCHING CHARACTERISTICS** (C_L = 50 pF, T_A = 25°C)

Characteristic		Figure	Symbol	V_{DD}	Typ #	Max	Unit
Output Rise Time	NAND, NOR	2, 3	t_{TLH}				ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns				5.0	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns				10	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns				15	65	130	
Output Fall Time	NAND, NOR	2, 3	t_{THL}				ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns				5.0	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns				10	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns				15	40	80	
Output Rise Time	NOR-Inverter	3	t_{TLH}				ns
t_{TLH} = (1.35 ns/pF) C_L + 32.5 ns				5.0	100	200	
t_{TLH} = (0.60 ns/pF) C_L + 20 ns				10	50	100	
t_{TLH} = (0.40 ns/pF) C_L + 17 ns				15	40	80	
Output Fall Time	NOR-Inverter	3	t_{THL}				ns
t_{THL} = (0.67 ns/pF) C_L + 26.5 ns				5.0	60	120	
t_{THL} = (0.45 ns/pF) C_L + 17.5 ns				10	40	80	
t_{THL} = (0.37 ns/pF) C_L + 11.5 ns				15	30	60	
Propagation Delay Time	NAND	2	t_{PLH},				ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 45 ns			t_{PHL}	50	130	260	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 37 ns				10	70	140	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 25 ns				15	50	100	
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 30 ns	NOR	3	t_{PLH},	5.0	115	230	ns
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 32 ns			t_{PHL}	10	65	130	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 20 ns				15	45	90	
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 45 ns	NOR-Inverter	3	t_{PLH},	5.0	130	260	ns
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 37 ns			t_{PHL}	10	70	140	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 25 ns				15	50	100	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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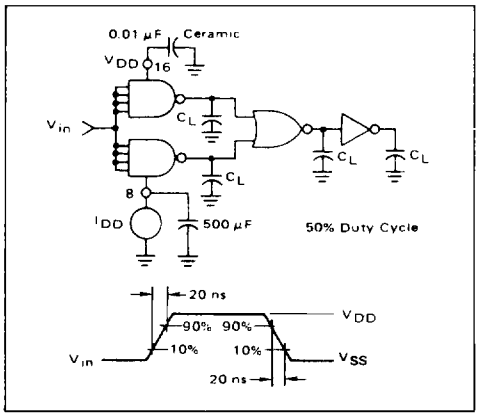
FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



PIN ASSIGNMENT

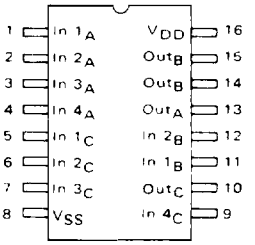


FIGURE 2 – 4-INPUT "NAND" GATE SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

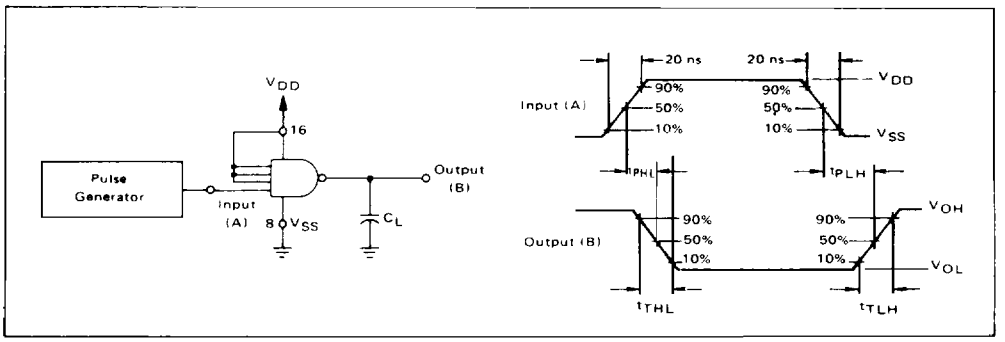
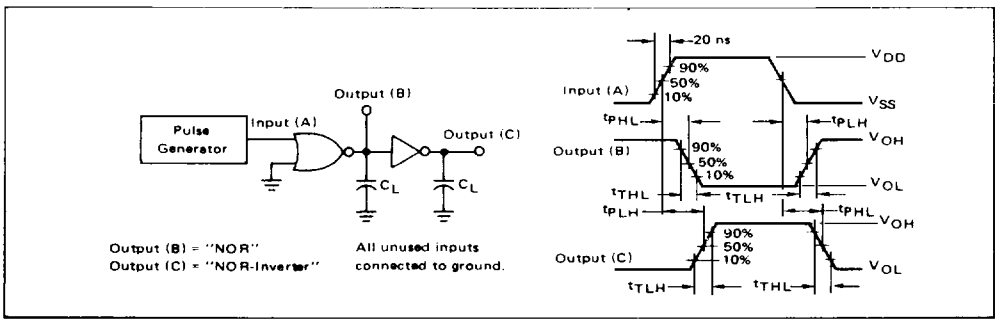


FIGURE 3 – "NOR" GATE and "NOR-INVERTER" SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



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