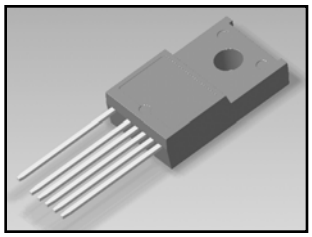
Allegro MicroSystems, Inc. SanKen

# Product Information

# *Series STR-W6200D*
# *PWM Off-line Switching Regulators*



## INTRODUCTION

The STR-W6200D series are current-mode PWM ICs that incorporate controller chips, made by a high-voltage proprietary BCD process, and avalanche-guaranteed MOSFETs. These elements allow power supply systems designs that are highly reliable and simple, with fewer peripheral components. These ICs also provide auto-burst mode operation, lowering input power requirements at light loads, and improving efficiency over the entire load range and universal-input range.

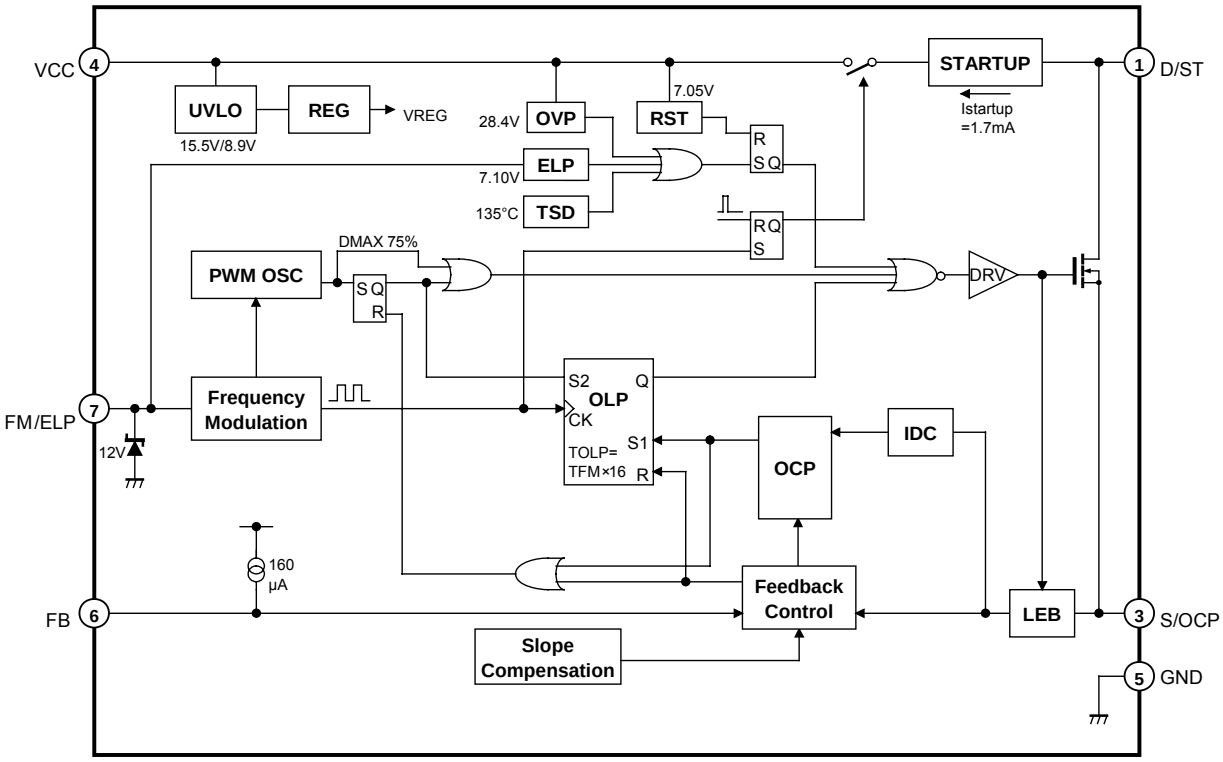
### Features

- TO-220 full-molded package with 6 pins
- 67 kHz PWM with frequency jittering operation for reducing EMI noise
- Overcurrent protection (OCP) with AC input voltage compensation function; no additional peripheral circuits required— minimizes dependency of OCP on AC input
- Overload protection (OLP) with integrated timer reduces power stress (temperature rise) at overload condition, requires no peripheral components
- Externally-activated shut down protection (External Latch Protection) for emergency system shut down
- Auto-burst standby function (pin < 0.1 W at zero output load condition)
  - Normal load (operation) ⇒ PWM mode
  - Light load (standby) ⇒ Burst mode (intermittent burst mode)
- Audible noise reducing function in Standby mode
- Avalanche-guaranteed MOSFET improves device capability to withstand excess surge voltage, providing a simple surge absorber circuit without breakdown voltage derating
- Start-up circuit eliminates the need for a start-up resistor, and helps to reduce input power consumption
- Bias Assist function improves start-up performance by self-biasing the VCC pin, and allows a use of a small value VCC capacitor, resulting in improved response to overvoltage conditions
- Very low current consumption in nonoperating (UVLO) state: $I_{CC(off)}$ = 5 µA (typ.) at $V_{CC}$=13.5 V
- Slope compensation circuit stabilizes operation, preventing interference from subharmonics
- Leading Edge Blanking
- Various protections:
  - Over Current Protection (OCP), pulse-by-pulse sensing
  - Over Load Protection (OLP), auto restart after certain duration
  - External Latch Protection (ELP), latched
  - Over Voltage Protection (OVP), latched
  - Thermal Shut Down (TSD), latched

All performance characteristics given are typical values for circuit or system baseline design only and are at the nominal operating voltage and an ambient temperature of 25°C, unless otherwise stated.

### Contents

## FUNCTIONAL BLOCK DIAGRAM




## TERMINAL ASSIGNMENTS

| Number | Name | Description | Functions |
|---|---|---|---|
| 1 | D/ST | Drain terminal | MOSFET drain, and input of startup circuit |
| [2] | – | [Pin removed] | – |
| 3 | S/OCP | Source/OCP terminal | MOSFET source, and overcurrent protection |
| 4 | VCC | Power supply terminal | Input of power supply for control circuit, and Over Voltage Protection |
| 5 | GND | Ground terminal | Signal ground |
| 6 | FB | FB terminal | Feedback signal input |
| 7 | FM/ELP | FM/ELP terminal | Capacitor connection terminal for frequency jitter modulation and External Latch Protection |



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## TERMINALS FUNCTIONAL DESCRIPTION

### VCC terminal (# 4)

The VCC terminal is the power source of the IC. It is connected to the constant-current source (1.7 mA typical) output of the start-up circuit, an input of which is connected to the drain terminal (D/ST, #1) of the IC. During the start-up process, the constant-current charges C2 at the VCC terminal (see figure 1), and when it reaches the start-up voltage (15.5 V typical), the IC starts switching operation. Hence, the C2 value decides the duration of the start-up period, as described by the following formula:

$$t_{startup} = C_2 \times \frac{V_{CC(on)} - V_{CC(init)}}{I_{startup}} \quad (1)$$

where $t_{startup}$ (s) is the start-up period, and $V_{CC(init)}$ is the initial voltage of VCC terminal. In general applications, $C_2$ should be 10 to 47 µF. After switching operation begins, the start-up circuit turns off, to zero its current consumption.

Figure 2 shows the relationship of VCC voltage and $I_{CC}$ (input current at the VCC terminal). As it shows, $V_{CC}$ has hysteresis between the IC start-up voltage (15.5 V typical) and UVLO (8.9 V typical). (Note: $I_{CC}$ is maintained very low under UVLO; for example, 5 µA typical at $V_{CC}$ = 13.5 V.)

After the IC starts operation, a voltage from an auxiliary winding (D in figure 1) becomes a power source to drive the IC, and VCC provides constant voltage. Figure 3 shows the VCC voltage behavior during the start-up period. The voltage of winding D goes up after the IC begins operation, and at some point, it overcomes the voltage drop of the VCC terminal due to power consumption out of the VCC capacitor, C2, reaching a certain voltage based on the turns ratio of the primary winding and winding D. To prevent activation of UVLO in cases where the voltage drop of VCC is faster than the winding voltage rise, as soon as VCC becomes lower than 15.2 V typical, the Bias Assist function activates the start-up circuit to feed current to C2 and thus prevent start-up failure. The bias function maintains the $V_{CC}$ voltage constant, and thanks to this function, the use of small value C2 capacitor is allowed, resulting in improved response for OVP (overvoltage) protection.

After the power supply properly starts up, VCC voltage fluctuates with positive dependency on the output power of the power supply (see figure 4). Therefore, the power supply must be designed in a way that ensures that the VCC voltage stays within UVLO and OVP trip voltage levels. A cause of this change is a

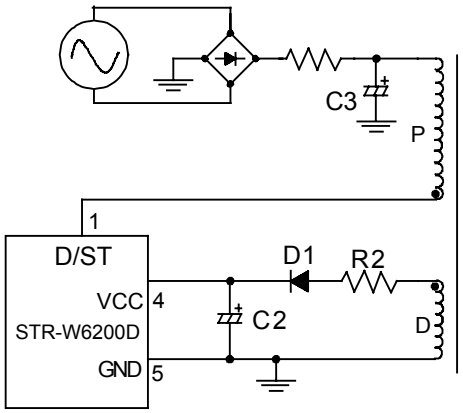


**Figure 1. Start-up circuit**

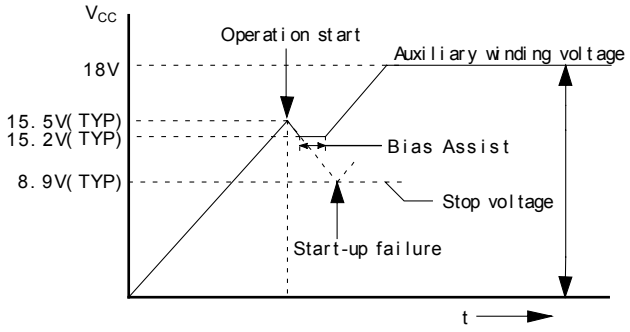


**Figure 3. $V_{CC}$ (C2) behavior at start-up**

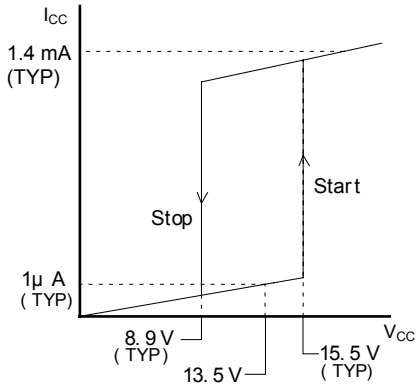


**Figure 2. $I_{CC}$ versus $V_{CC}$**

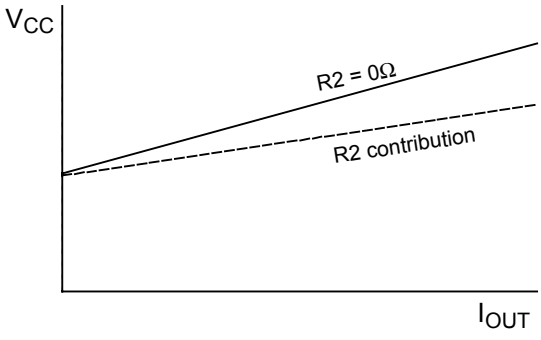


**Figure 4. $V_{CC}$ versus $I_{OUT}$**



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leakage inductance of the transformer. The leakage inductance leads to a surge voltage on the drain (D/ST) terminal when the MOSFET turns off. Because it is coupled to the D winding, it ultimately affects VCC voltage. Therefore, minimizing the leakage inductance is a primary design concern, and it is done by improving the coupling between the primary winding and the regulated secondary winding. In addition, lowering the effects of the drain surge voltage on winding D is accomplished by loosing the coupling of winding D and the primary winding, and tightening the coupling of D and the regulated-secondary winding. All of the above measures are aspects of the transformer structural design, described below as design suggestions. Another measure is the use of R2 (see figure 5), with a value, in general, of up to several tenths of an ohm.

Here are commonly used techniques to minimize VCC voltage fluctuation:

- Target voltage setup of the winding D: choose the turns of winding D to attain a $V_{CC}$ of 15 to 20 V
- Transformer structure:
  - sandwich the primary winding and the regulated secondary winding for minimizing inductance leakage
  - position winding D away from the primary winding, and close to the regulated secondary winding. For example, sandwich winding D with the regulated secondary winding
  - Another measure is stacking coils as follows, (from the bottom to the top of the transformer bobbin): half-primary winding → regulated secondary winding → winding D → regulated secondary winding → half-primary winding

3) Series resistor R2 (simplest method): in a typical application, the value should be up to several tenths of an ohm.

4) Determine all of the factors above based on an actual experiments, in order to make sure that VCC voltage stays within: $V_{CC(OFF)} < V_{CC} <$ OVP (min.); where $V_{CC(OFF)} = 9.8$ V (max), and $V_{CC(OVP)} = 27.0$ V

### About PWM operation

The IC is a PWM switcher with an operating frequency of 67 kHz. The timing pulse (set pulse) used to turn on the MOSFET is generated by the PWM OSC circuit.

### Operation at start-up, S/OCP terminal (#3)

$V_{R1}$ is the voltage across the drain current sensing resistor, R1. After passing through the S/OCP terminal (#3), it is compensated by the IDC circuit, then input into the OCP circuit, which turns off the MOSFET at the threshold voltage, $V_{OCP} = 0.9$ V typical. After a certain period of time passes, the set pulse of PWM OSC turns on the MOSFET again. These operations repeat during the start-up period until the closed loop feedback system starts working.

### Constant output voltage control at steady operation, FB terminal (#6)

The output voltage control uses a negative current mode closed loop feedback system for stable operation, and feedback current is input at FB terminal (#6) from the opto-coupler. This feedback current increases at light load condition, and decreases at heavy load condition. Based on the feedback current, there is a certain voltage created at the FB terminal that is added with the voltage of the slope compensation signal and input to FB comparator as a target conditional voltage. The FB comparator compares it with the input signal of $V_{R1}$. This entire system creates the current mode closed loop feedback system. (See figure 6.)

Figure 7 shows the drain current waveform in subharmonic oscillation. This is a theoretically occurring phenomenon for a drain current peak-detection control method, and it creates a drain current pulse fluctuation with even multiples of a fundamental operating frequency, especially when the power supply operates in continuous operating mode. In continuous operating mode, the drain current forms a trapezoidal waveform, and even if the target drain peak current is constant in steady output load condition, the drain current width can vary. It is affected by the

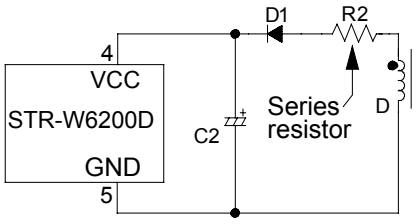


**Figure 5. VCC peripheral circuit with R2**

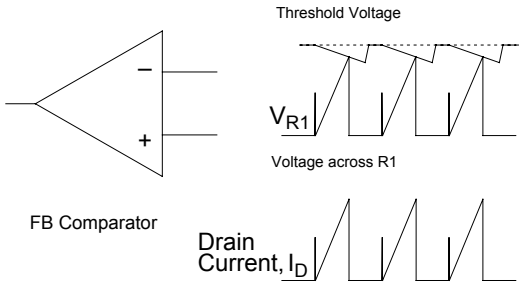


**Figure 6. Operation of FB comparator**

first drain current width as depicted in figure 7, and the closed feedback loop cannot stabilize a proper amount of drain current adjustment within one PWM cycle, but instead takes several cycles.

Slope compensation is made to create a steady cycle PWM operation, and it superimposes the down-slope signal on the FB terminal voltage, which creates a signal negatively proportional to the drain current width increase in a way that reduces the drain peak, and suppresses the subharmonic oscillations.

In general applications, a surge voltage occurs, resulting from a drain surge current when the MOSFET turns on. In order to prevent the OCP comparator from responding to this, the leading edge blanking ($t_{hw}$ = 400 ns) is integrated, turning off the MOSFET irregularly.

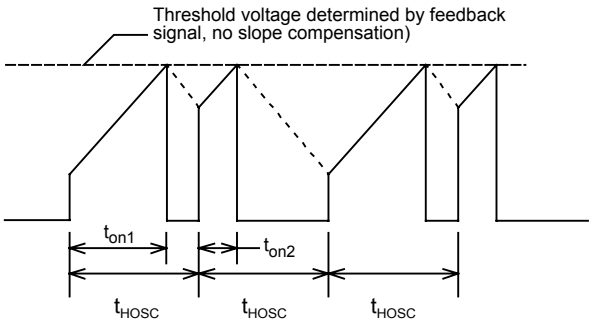


**Figure 7. Drain current, $I_D$, waveform in subharmonic oscillation**

### Frequency Jitter, FM/ELP terminal (#7)

The jittering function helps to reduce the conduction of EMI noise and consequently contributes to the reduction of EMI filtering costs. The IC integrates the frequency jittering function, as shown in figure 8 drain voltage and current waveforms, with an average frequency of 67 kHz and an internally-fixed fluctuation width of $\Delta f \approx 6.9$ kHz typical.

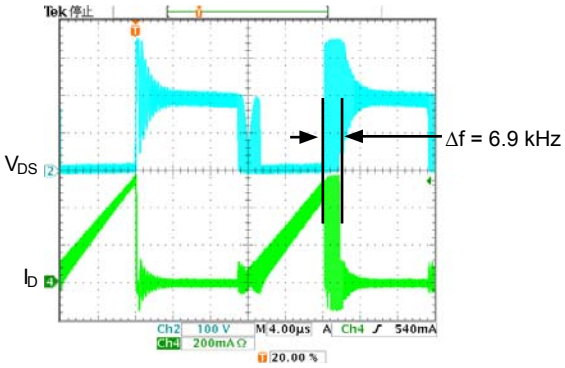


**Figure 8. Jittering in the $V_{DS}$ and $I_D$ waveforms**

Figure 9 shows FM/ELP (terminal #7) voltage and jittering cycle. The jittering cycle (modulation rate) is determined by the value of capacitor C3 at terminal 7. The IC internal sink ($I_{sink(FM)}$ = 13 µA typical), and source ($I_{sorc(FM)}$ = 13 µA typical) constant-current sources repeatedly charge and discharge C3 between 2.8 and 4.5 V, to create the triangular shape. The PWM oscillator uses this signal to create the jittering modulation, and therefore the jittering modulation cycle, $t_{FM}$, can be adjusted by the value of C3. The value of $t_{FM}$ (s), can be determined by the following formula:

$$t_{FM}(s) = 2\left(\frac{C_3 \times \Delta V_{FM}}{I_{sink/sorc(FM)}}\right) = 2\left(\frac{C_3(\mu F) \times 1.7(V)}{13\ \mu A}\right) \quad , \qquad (2)$$

where the modulation frequency, $f_{FM}$ (Hz) = $1/t_{FM}$, and $C_3$ is the capacitance, expressed in µF. In general, a $C_3$ value in the range of 0.015 to 0.047 µF is recommended.

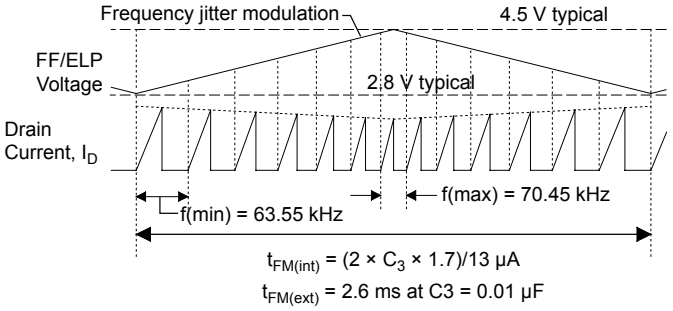


**Figure 9. FM/ELP terminal voltage and jittering cycle**



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### Overcurrent Protection with AC Input Compensation, S/OCP terminal (# 3)

The overcurrent protection (OCP) circuit detects each drain peak current (pulse-by-pulse method), and limits the output power of the power supply. This circuit integrates the AC input compensation circuit (IDC) to minimize deliverable output power dependency on AC input voltage level, without requiring any external additional components.

Figure 10 shows the deliverable output power dependency on AC input voltage. In conventional power supplies, the drain peak tends to overshoot its overcurrent limiting point because of the time delay between overcurrent detection and actual MOSFET turn-off. This results in a gap of deliverable output power points between low AC input and high AC input. In order to minimize this power gap, the IDC circuit creates a compensated overcurrent threshold signal in reference to duty cycle, ON Duty, as depicted in figure 11, and superimposes it on the S/OCP (terminal #3) input signal.

Figure 12 shows the overcurrent threshold point, compensated by this function, which works in a way to raise the deliverable output power of the low AC input voltage to the high AC input voltage. Also, as figure 12 shows, the overcurrent threshold point reaches 0.875 V when a transformer is designed to have a 50% duty cycle at maximum output power and minimum AC input voltage (85 V).

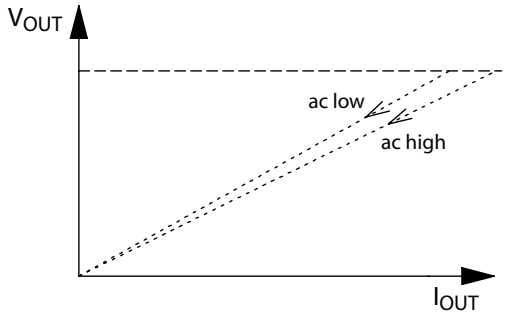


**Figure 10. VOUT versus-IOUT (secondary)**

$$V_{OCP2}\,(\mathrm{V}) = V_{OCP1}\,(\mathrm{V}) + D_{PC} \times ONDuty\,(\%)\ ,$$

where $D_{PC}$ is in mV / ONDuty (%), with the value range from 1.5 (min.), 1.9 (typ.), to 2.3 (max.).

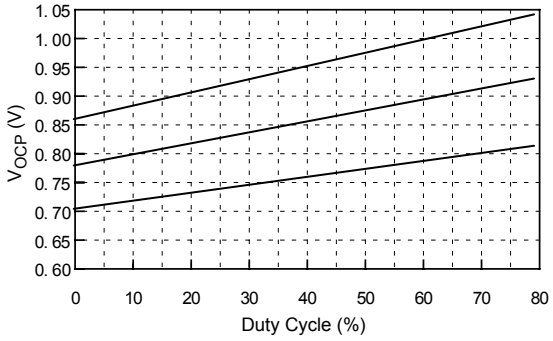


**Figure 11. Duty Cycle versus OCP threshold voltage; formula with results charted**

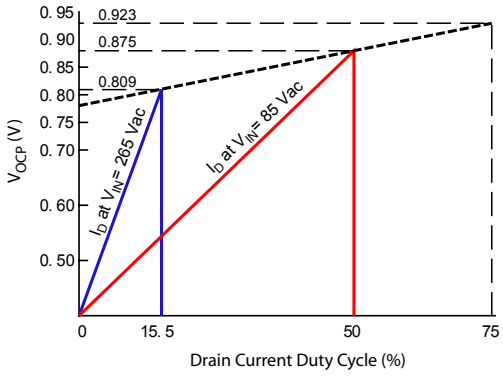


**Figure 12. $I_D$ Duty Cycle versus OCP threshold voltage**

### Overload protection, FM/ELP terminal (#7)

The overload protection (OLP) circuit is activated when over-current protection (resulting from abnormal output load condition) is inactive for a certain period, $t_{DLY}$. It then stops switching operation. After that, OLP it is released (auto-restart) when the abnormal load condition is removed. Figure 13 shows the waveforms of the drain current, FM/ELP terminal voltage, and VCC terminal voltage during OLP and the auto-restart event. Figure 14 shows peripheral circuits used to implement OLP.

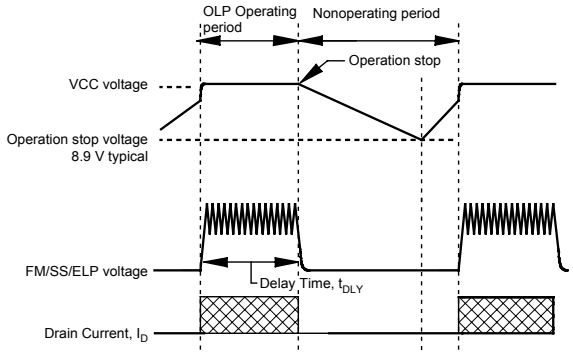


**Figure 13. Waveforms during OLP**

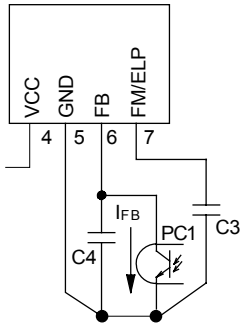


**Figure 14. OLP implementation schematic**

The value of $t_{DLY}$ is equal to 16 times the charge-discharge cycle of C3 (shown in figure 14), and its formula is:

$$t_{DLY}\ (typ.)(s) = t_{FM} \times 16 \quad (3)$$

$$t_{FM}\ (typ.)(s) = \frac{2 \times C_3\ (\mu F) \times 1.7(V)}{13\ (typ.)(\mu A)} \quad (4)$$

where $t_{FM}$ is determined by equation 2, and $C_3$ is the capacitance.

After OLP is activated, the switching operation is stopped, and therefore VCC voltage drops until it eventually reaches the UVLO voltage, 8.9 V. After this, the power supply status returns to the start-up initial conditions, except the initial VCC voltage because of residual voltage on the VCC capacitor. VCC voltage rises due to the start-up circuit action, and the power supply restarts switching operation as soon as VCC voltage reaches $V_{CC(ON)}$ = 15.5 V. At that point, unless the abnormal condition is removed, the power supply stops switching operation again. This intermittent switching operation is repeated until the abnormal condition is removed, at which time the power supply returns to normal operation.

The OLP circuit protects the power supply in case the winding D voltage does not drop at abnormal output load conditions because of poor coupling of a transformer. A key design point is that the C3 value chosen must ensure that $t_{DLY}$ is longer than the period from the beginning of switching operation to the point of steady operation, or more precisely, to the starting point of the opto-coupler feedback current, when the power supply starts. Otherwise, if $t_{DLY}$ is too short, the power supply fails to start up. In general, a value of 0.01 to 0.047 µF is recommended for C3 value, and the optimal value should be decided by actual experiments.

### Auto Burst Mode, FB terminal (#6)

The Auto-Burst function is activated at approximately 15% of the maximum drain peak current, $I_D$. Figure 15 shows the drain current and output load current. When the drain peak current drops to about 15% of its maximum value at light output load condition, the Feedback Control circuit stops switching operation. This leads to the output voltage dropping, reduction of the feedback current, and the Feedback Control circuit releasing the switching operation. After this, as switching continues, the

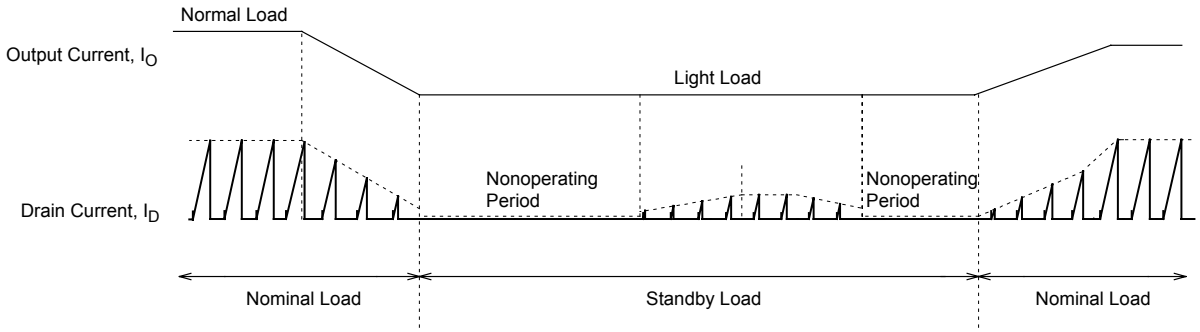


**Figure 15. Auto-Burst timing chart**



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feedback current increases again, and the process repeats. In addition, during this process the 15% of the drain peak current minimum level reduces audible noise from a transformer.

### Latch circuit

The Latch circuit is linked to the overvoltage (OVP) and thermal shut down (TSD) protections, and it has a delay circuit of 10 µs to avoid irregular activation from noise interference. The internal regulator circuit is kept on even if the Latch circuit is on, and it maintains a certain level of IC operational input current. This current reduces VCC voltage during latching, and UVLO is activated. Eventually, the power supply returns to start-up status. The Latch circuit is not released during UVLO, and therefore, even if VCC reaches $V_{CC(ON)}$ = 15.5 V (normally sufficient to start IC operation), switching operation does not start and VCC voltage drops, again. This repeats, as shown in figure 16, and prevents VCC voltage excess increase.

Releasing the latch is done by dropping the VCC voltage below $V_{CC(La.Off)}$ = 7.1 V typical, which is normally done by shutting off AC input.

### External latch protection (ELP)

This function shutdowns IC operation when more than 7.1 V typical (the external latch protection threshold voltage) is applied to the FM/ELP terminal (#7). To ensure proper activation, a current source in the range of 100 µA to several milliamperes is recommended to pull up the terminal. The terminal has a 12 V clamp Zener diode inside the IC to clamp further voltage increase. The application circuit in figure 22 shows the circuit example of the use of the opto-coupler for this function.

### Thermal shut down (TSD)

Thermal shut down is activated when an internal frame temperature of 135°C is linked to the latch.

### Overvoltage protection (OVP)

This feature protects output loads and circuits against excess voltage occurring at the power supply outputs due to an open loop condition. It is done by sensing VCC voltage, and when it reaches $V_{CC(OVP)}$ = 28.5 V typical, it is linked to the latch. The formula below determines the output voltage used to activate the overvoltage protection:

$$V_{OUT(OVP)} = \frac{V_{OUT}}{V_{CC}} \times 28.5\ \text{V (typ.)} \quad , \qquad (5)$$

where $V_{OUT}$ and $V_{CC}$ are the voltage levels during normal operation.

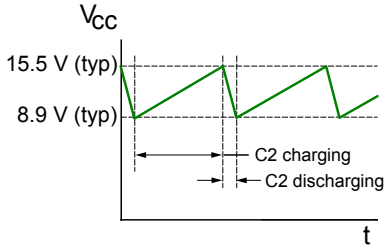


**Figure 16. VCC terminal voltage at latch**

## APPLICATION INFORMATION

### External components

Use properly rated, including derating, and proper type of components.

- Input and output electrolytic capacitors. Apply proper derating against ripple current, and voltage and temperature rise. Use of high ripple current and low impedance types, designed for switch mode power supplies, is recommended.
- Transformer. Apply proper derating against core temperature rise from core loss and copper loss.
- Current sensing resistor R1. Choose a low inductance and surge-proof type

### Transformer design

Because switching current contains a high-current component, the skin effect becomes significant. Therefore, wire gage should be decided based on rms current and current density of 3 to 4 A per $mm^2$. In case temperature rise becomes an issue, consider the following measures:

- increasing the number of wires
- using litz wire
- increasing wire diameter.

### Phase compensation

Figure 17 shows a typical phase compensation circuit with a secondary shunt regulator. A value for C6 of 0.047 to 0.47 µF is recommended. Figure 18 shows C4 at the drive winding to the primary circuit for reinforcing the phase compensation to avoid irregular operation due to special load conditions, secondary large ripple currents, or noise interference to the FB terminal (#6). A C4 value of 470 pF to 0.01 µF is usually recommended.

### Capacitance of C3 at the FM/ELP terminal (#7)

The capacitor C3 at the FM/ELP terminal (#7) determines the jittering frequency, $f_{FM}$, and the OLP delay time $t_{DLY}$. Figure 19 shows the relationship between them and the C3 value. A C3 value of 0.01 to 0.047 µF is recommended, although the proper value should be determined by actual experiments.

### Maximum duty cycle and transformer design

The slope compensation circuit is integrated as a measure of sub-harmonics, and it provides steady operation at more than 50% duty cycle and trapezoidal drain current shape.

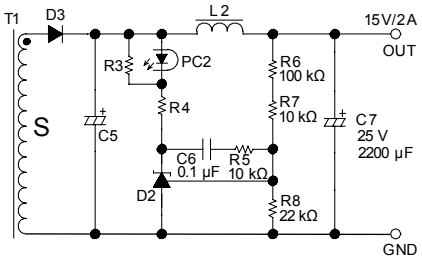


**Figure 17. Using C6 for phase compensation**

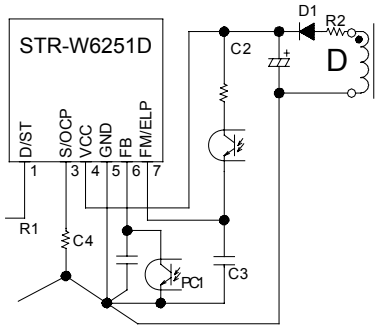


**Figure 18. Using C4 for phase compensation**

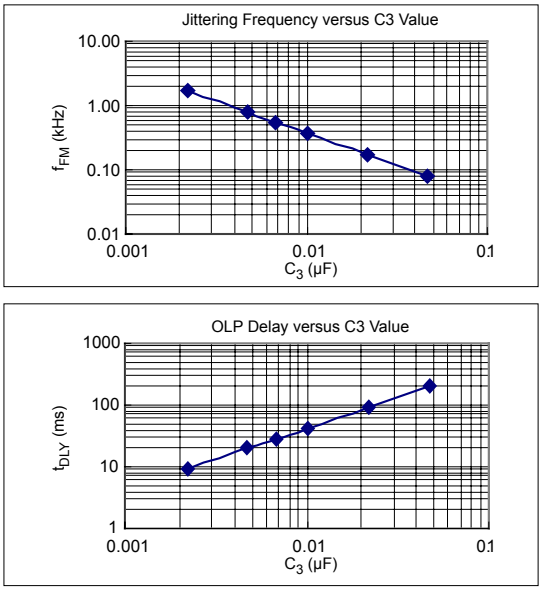


**Figure 19. Using C3 for setting $f_{FM}$, $t_{ss}$, and $t_{DLY}$**



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### EMI measure of secondary diode

Panel A of figure 20 shows a ordinal method (Cdi) to reduce EMI noise from the secondary diode. However, it sometimes causes irregular ringing of the drain current, thus, in case it happens, use of a damper resistor, Rdi, is recommended (see panel B). In this case, temperature rises of these components should be monitored.

### Component layout and pattern design

- Pattern of S/OCP terminal - R1 - C3- Winding P1 (transformer) - D/ST terminal

This pattern contains switching current, and it should be wide, short, and its loop length less than 150 mm. In case the distance between C3 and the IC becomes long, intermittent capacitors near both the IC and the transformer is recommended. The capacitors may be either electrolytic or film type capacitors, with values in the range 0.1 µF / 200 to 400 V).

- Pattern of GND terminal - (–)C2 - Winding D (transformer) - R2 - D1 - (+) C2 – VCC terminal

This pattern also needs to be as wide and short as possible, and a loop length of less than 180 <mm is recommended. In case the VCC terminal and C2 are not close, placing a film capacitor of 0.1 µF / 50 V) between the VCC and GND terminals is recommended.

- R1 and GND pattern

Place R1 as close as possible to S/OCP terminal. There should be a single point ground (A in figure 21) between the power ground circuit and the control circuit to avoid interference of switching current to the control circuit.

### Other precautions

- SMPS (switching mode power supply) peformance. Pattern design and component layout affects proper functioning during operation, EMI noise, and power dissipation. Therefore,

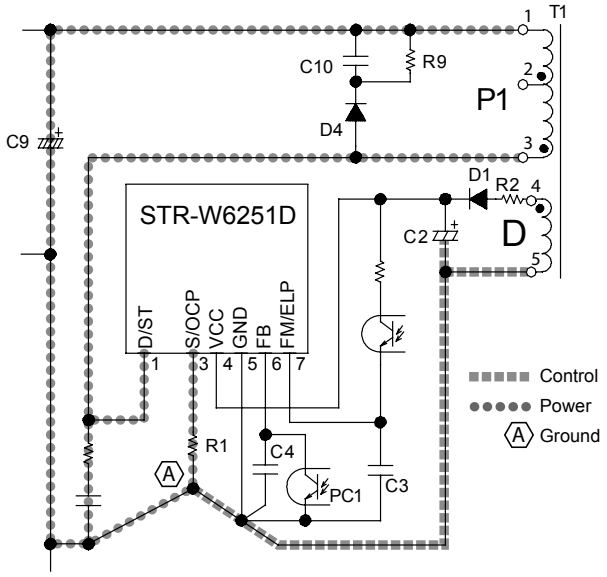
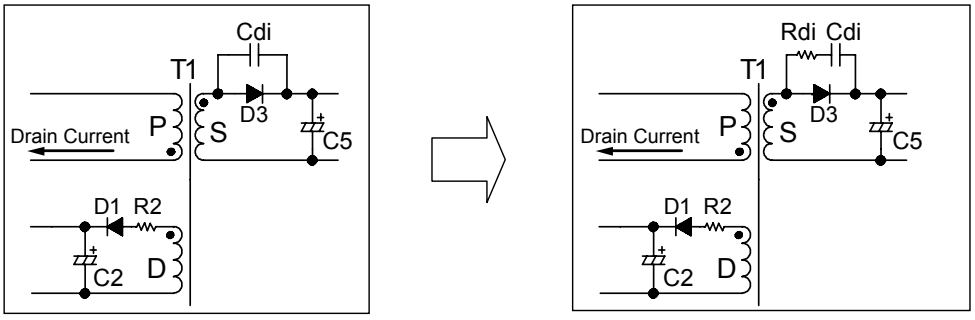



**Figure 21. Peripheral component grounding**




**(A)** **(B)**

**Figure 20. EMI measure circuits: (a) ordinal method of measurement, (b) measurement with a damper resistor, Rdi**



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where high freqeuency current runs, wide, short patterns and small circuit loops are imporntant. In addition, GND and earth patterns affect radation EMI noise, thus the same measures should be taken into account.

- Safety guidelines. Pattern design and component layouts should be done to comply with all safety guidelines.
- MOSFET. When using a MOSFET, as in the circuit shown in figure 21, take into account the positive thermal coefficient of $R_{DS(ON)}$ when preparing your thermal design.

## APPLICATION CIRCUIT

Design considerations:

- For improving heat dissipation, as large a pattern as possible from the D/ST pin is recommended.
- In case of large surge voltages on the D/ST pin, use of a snubber circuit across the primary winding or damper circuit between the D/ST pin and GND is recommended.

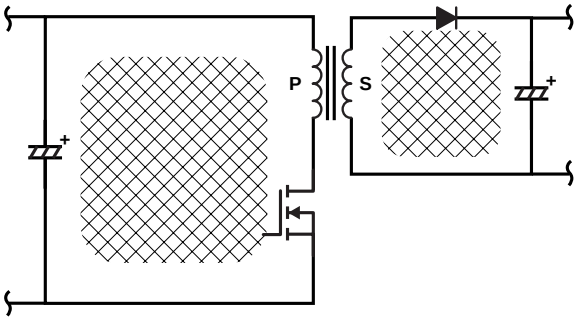


**Figure 23. Layout for high-frequency, high-current loops; place components within loop (in hatched area) to minimize lengths of traces**

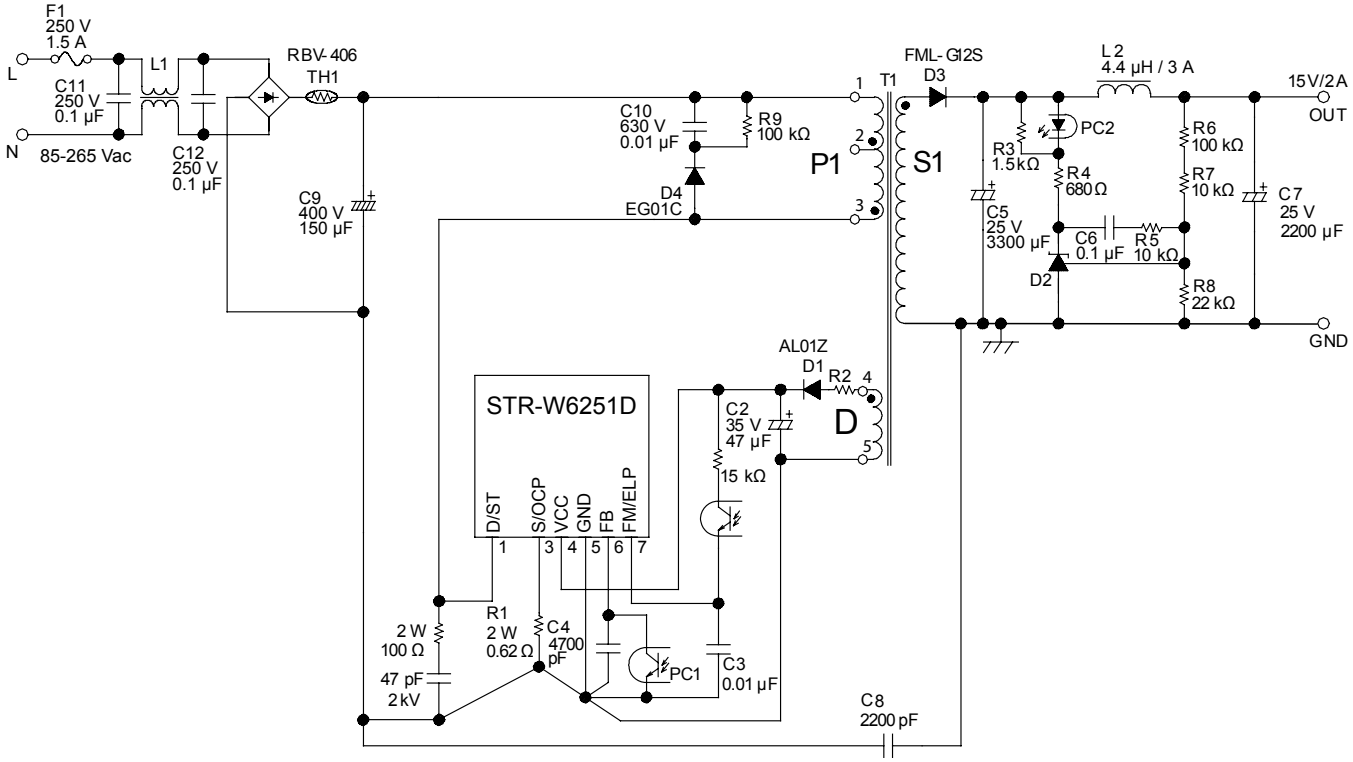


**Figure 22. Typical application circuit**



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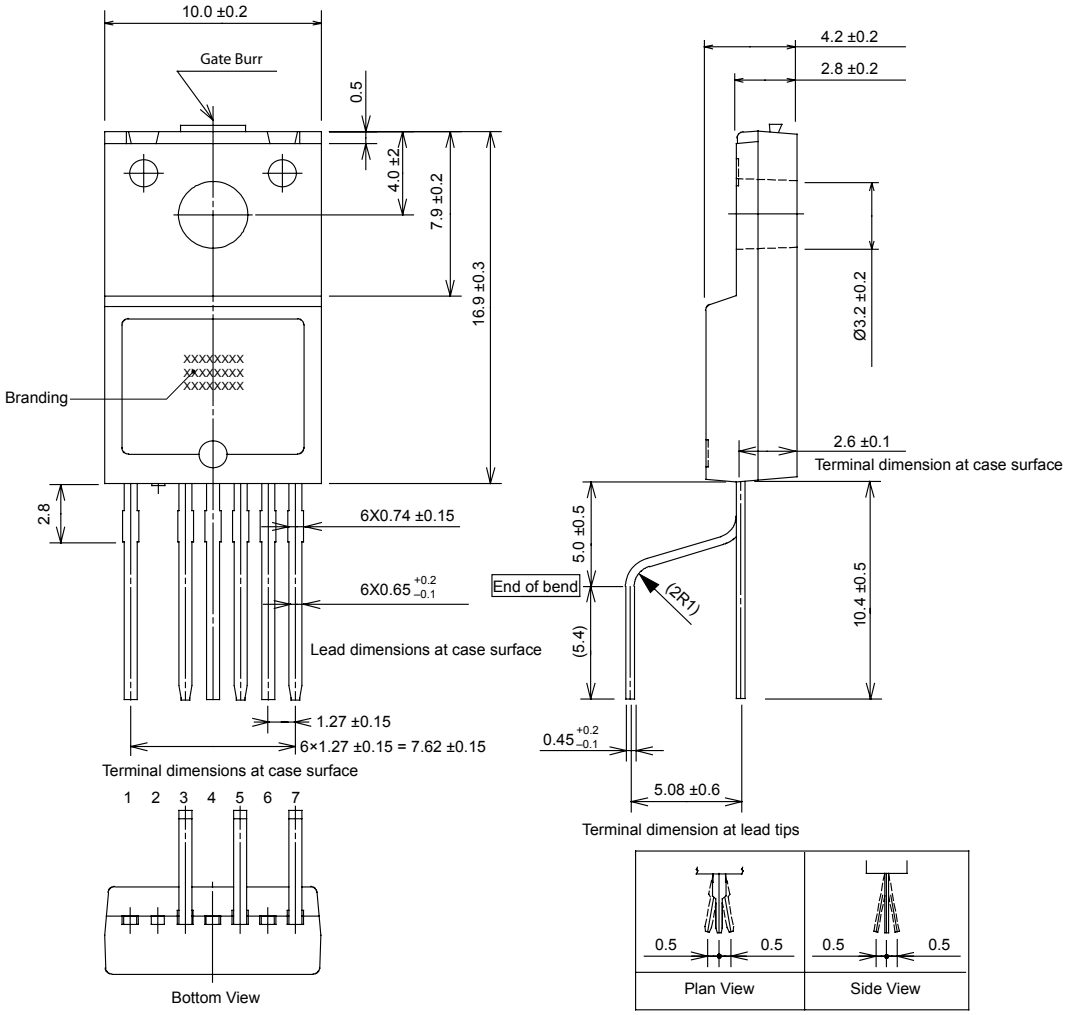
## PACKAGE OUTLINE DRAWING

The following example is an STR-W6251, leadform 2003




Terminal core material: Cu
Terminal treatment: Ni plating and solder dip
Weight: approximately 2.3 g
Leadform: 2003

Dimensions in millimeters

Branding:
1st line, Family: STR
2nd line, Type: W6251
3rd line, Lot: *YMDD*

Where: Y is the last digit of the year of manufacture
M is the month (*1* to *9*, *O*, *N*, *D*)
DD is the 2-digit date



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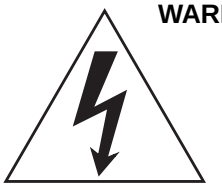

**WARNING** — These devices are designed to be operated at lethal voltages and energy levels. Circuit designs that embody these components must conform with applicable safety requirements. Precautions must be taken to prevent accidental contact with power-line potentials. Do not connect grounded test equipment.

The use of an isolation transformer is recommended during circuit development and breadboarding.

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