APPLICATION NOTE

Application information for TDA8359J deflection output circuit

AN 00039

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Keywords

TDA8359J
Vertical deflection
Field
Monitor
90°, 110°
4 : 3, 16 : 9

Date: augustus 2000

Summary

In this report you can find an application and product description of the DC coupled deflection output circuit with the type number TDA8359J. The TDA8359J is functional the same as the TDA8357J but is able to deliver a higher output current. The application design procedure and the application investigations are given at the end of this report.

CONTENTS

LIST OF FIGURES

1. INTRODUCTION.

The TDA8359J is an integrated power circuit for use in 90° and 110° colour deflection systems. It contains a vertical deflection bridge output, operating as a high efficiency class G system and can handle field frequencies from 25 to 200 Hz. The vertical coil of a 4 : 3 as well a 16 : 9 picture tube can be connected to this vertical deflection device. Due to the bridge configuration a DC deflection output application can be designed with a positive main supply of typical 12 Volts and a positive flyback supply of typical 45 Volt. (Depending on the coil data).

This integrated circuit is designed in a Low Voltage DMOS (LVDMOS) process that combines bipolar, CMOS and DMOS components. DMOS output transistors (MOSFETs) are used because of the absence of secondary breakdown, which gives a better SOAR performance. The internal circuits are designed in such way that only a few external components are needed to get a correct working application.

The TDA8359J is functional the same as the TDA8357J vertical deflection output stage. The TDA8359J differs in only one aspect from the TDA8357J, it is able to deliver a higher output current which is more suitable for large picture tubes.

A detailed investigation procedure to determine an optimum application is given at the end of this report.

1.1 Features.

- Few external components required
- High efficiency fully DC coupled vertical bridge output circuit
- Short rise and fall time of the vertical flyback switch
- Picture tube burn in protection signal (guard circuit)
- Temperature (thermal) protection circuit
- Differential mode inputs
- Blanking pulse generator (guard)
- Improved EMC performance due to differential inputs

1.2 Ordering information.

Type Number	Package		
	Name	Description	Version
TDA8359J	DBS9P	plastic DIL-bent-SIL power package; 9 leads (lead length 12/11 mm); exposed die pad	SOT523-1

1.3 Block diagram

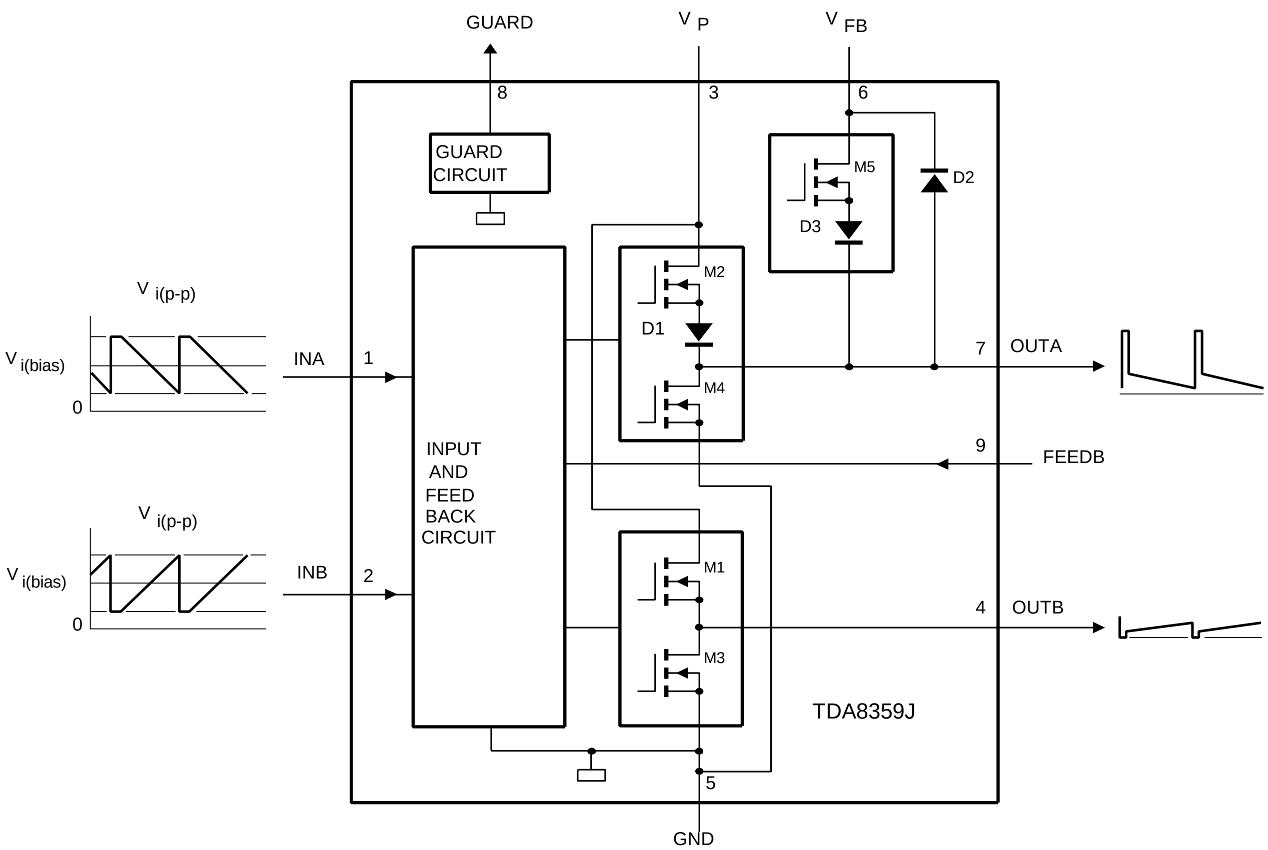
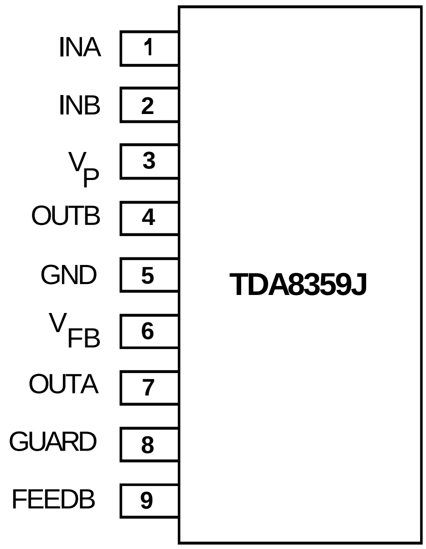


Fig 1: Blockdiagram.

1.4 Pinning

Symbol	Pin	Description
INA	1	input A
INB	2	input B
V_P	3	supply voltage
OUTB	4	output B
GND	5	ground
V_{FB}	6	flyback supply voltage
OUTA	7	output A
GUARD	8	guard output
FEEDB	9	feedback input



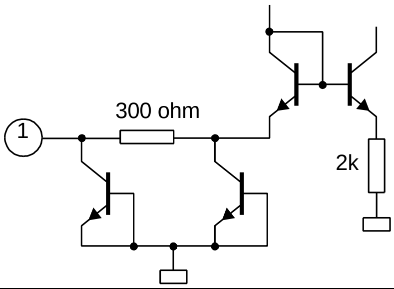
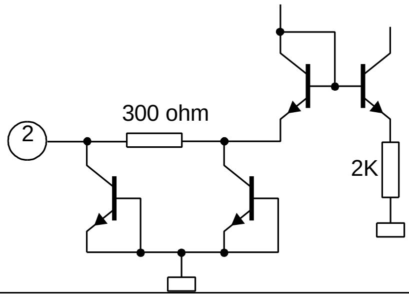
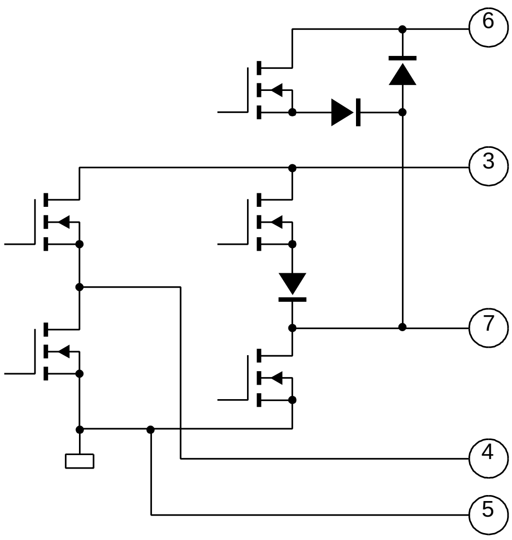
1.5 Quick reference data

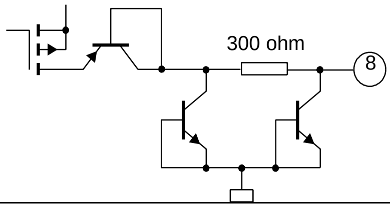
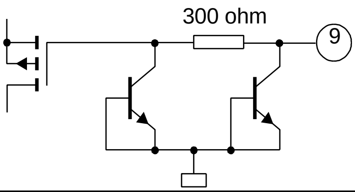
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Supplies						
V_P	supply voltage		7.5	12	18	V
V_{FB}	flyback supply voltage		$2xV_P$	45	66	V
$I_{q(P)(av)}$	average quiescent supply current	during scan	-	10	15	mA
$I_{q(FB)(av)}$	average quiescent flyback supply current	during scan	-	-	10	mA
P_{tot}	total power dissipation		-	-	8	W
Input and outputs						
$V_{i(dif)(p-p)}$	differential input voltage (peak-to-peak value)		-	1000	1500	mV
$I_{o(p-p)}$	output current (peak-to-peak value)		-	-	3.2	A
Flyback switch						
$I_{o(peak)}$	maximum (peak) output current	$t \leq 1.5$ ms	-	-	±1.8	A

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Thermal data; in accordance with IEC 747-1						
T_{stg}	storage temperature		-55	-	+150	°C
T_{amb}	ambient temperature		-25	-	+ 75	°C
T_j	junction temperature		-	-	+150	°C
$R_{th(j-c)}$	thermal resistance from junction to case		-	-	3.5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	-	-	65	K/W

2. DEVICE DESCRIPTION AND APPLICATION INFORMATION

2.1 Internal pin configuration

Pin	Symbol	Equivalent circuit
1	INA	
2	INB	
3	V_P	
4	OUTB	
5	GND	
6	V_{FB}	
7	OUTA	

Pin	Symbol	Equivalent circuit
8	GUARD	
9	FEEDB	

2.2 Application diagram

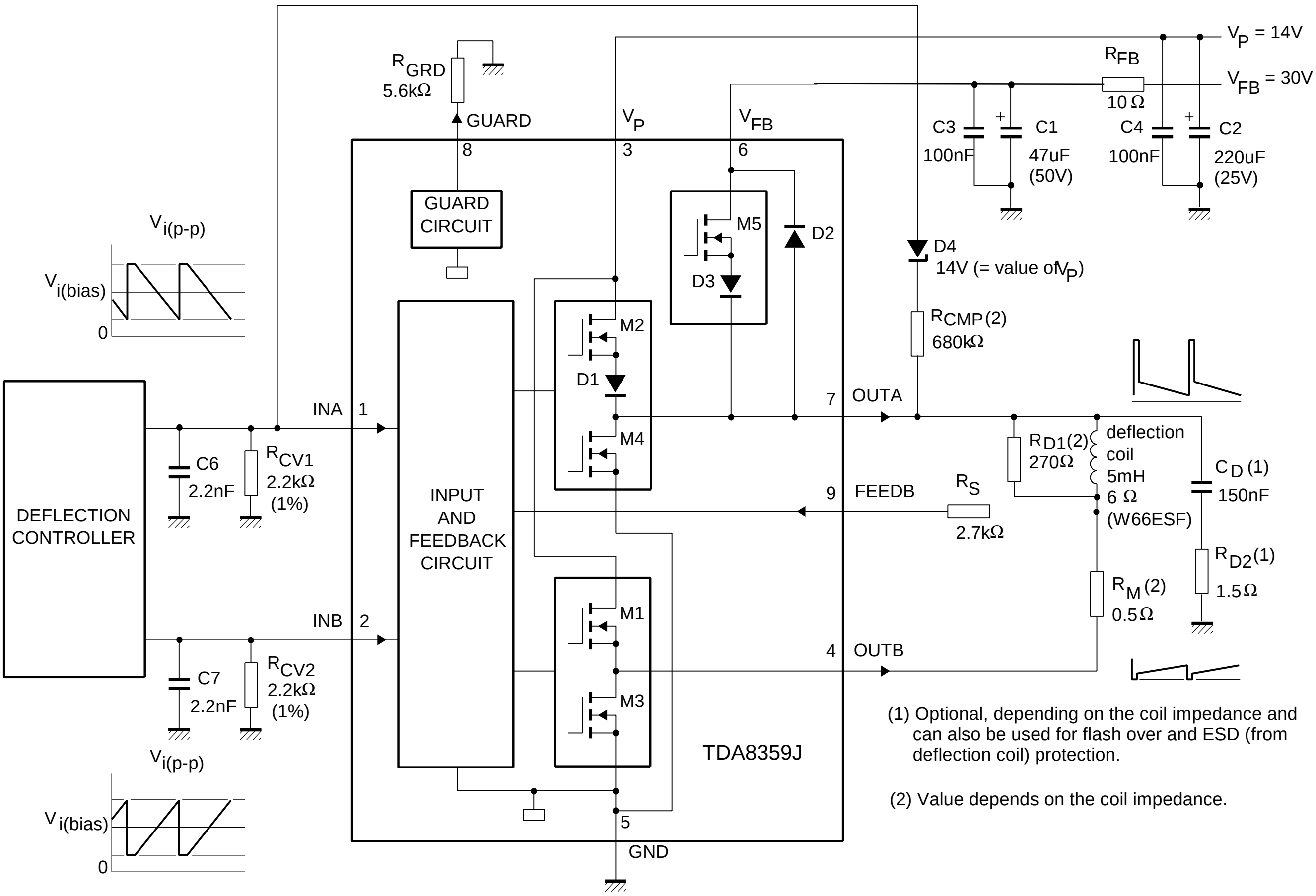


Fig 2: Application diagram.

The TDA8359J is a vertical drive circuit in a bridge configuration. The output amplifiers are driven in opposite phase.

When looking at the application diagram, the following components can be described in short terms (detailed information is given in the succeeding paragraphs).
The input circuit of the TDA8359J is a differential voltage input. The external resistors R_{cv1} and R_{cv2} convert the input currents into input voltages. The differential input voltage is compared with the voltage across the measuring resistor R_M that provides feedback information. The deflection coil is connected between OUTA and resistor R_M and OUTB.
The damping resistor R_{D1} is connected across the deflection coil for HF loop stability. The damping resistor compensation that consists of a resistor R_{CMP} in series with a zenerdiode D4, compensates current differences in the damping resistor during scan and flyback and assures a short settling time.

2.3 Vertical amplifier

In many conventional deflection output circuits, the deflection coil must be AC coupled. This will require an expensive coupling capacitor of approximately 2200 µF. Beside higher costs, the coupling capacitor can cause picture bounce after switching between channels on the tv set. This capacitor can be omitted in a DC coupled deflection output circuit.

The TDA8359J is a DC coupled deflection output circuit, which has no bounce effect during channel switching and has an improved EMC immunity. This is achieved by using differential mode inputs. The deflection coil and the measuring resistor R_M are connected between the output amplifiers of the TDA8359J that are driven in opposite phase. See Fig 3.

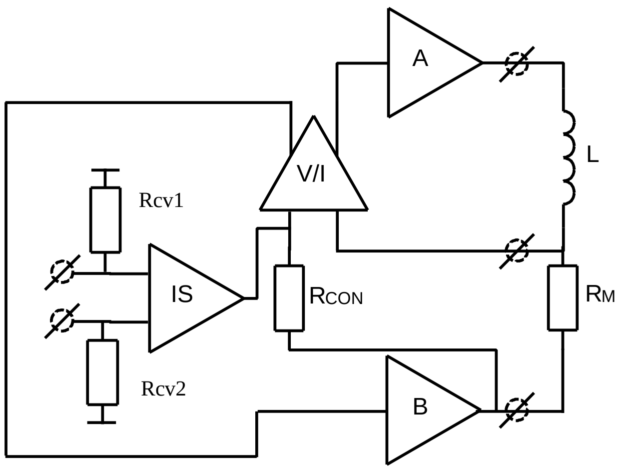


Fig 3: Simplified block diagram of the vertical circuit.

Since the Input Stage (IS) is voltage driven, resistor R_{cv1} and R_{cv2} are used when the driver circuit delivers a differential output current (See Fig 3) such as the Ultimate One Chip. So, driver circuits which deliver an output voltage can also be used, in that case resistor R_{cv1} and R_{cv2} are not necessary.

The voltage across the internal conversion resistor R_{con} is compared with the output current through the deflection coil (by means of a voltage current converter V/I), which is measured as a voltage across R_M.
The output amplifiers A and B will be driven until both voltages are equal. This means that the deflection current is determined by the ratio of the input resistors $R_{cv1,2}$ and the measuring resistor R_M.

The output current is adjustable from 0.5 $Ampere_{p\text{-}p}$ to 3.2 $Ampere_{p\text{-}p}$ mainly by varying resistor R_M. The maximum differential input voltage across $R_{cv1,2}$ is 1500 $milliVolt_{p\text{-}p}$ for each pin. The minimum input bias voltage is 100 mV, however a minimum input voltage of 300 mV is recommended because of a better linearity.

2.3.1 Vertical input circuit

The input circuit is suitable for direct connection to driver circuits, which deliver symmetrical (or asymmetrical) current signals. Some type numbers of suitable drive circuits: TDA9151B, TDA9160A, TDA9162, TDA933X, TDA8366, TDA8367, TDA837X, TDA884X, TDA885X (one chip family), TDA935X/6X/8X (ultimate one chip family) and TDA485X (deflection processor family).

An example of the vertical drive output signal of a “one chip” family IC is given below. (The drive signal depends on which drive circuit is used. In the ultimate one chip family, the zoom is standard enabled and is set to a value of 19 on a range of 0 – 63. This causes a small flat piece just before the start of the scan).

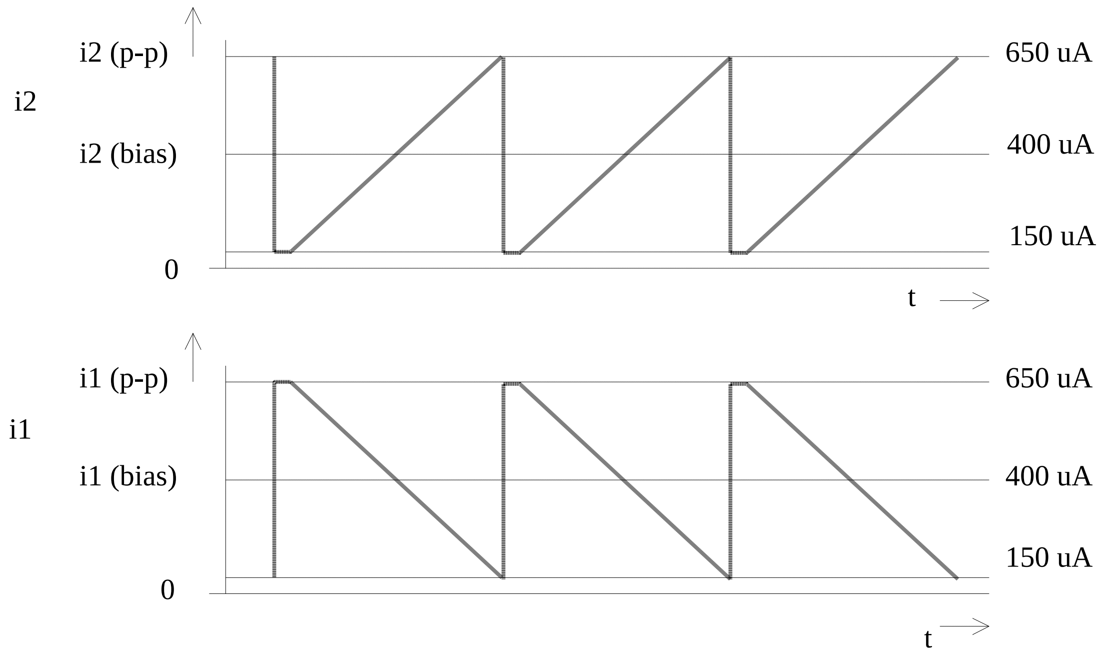


Fig 4: Vertical drive output currents of an onechip family IC.

The bias output signal current is 400 µA typical. The differential mode output current is typical 500 μA_{P-P} and maximum 600 μA_{P-P} .

After connecting an "ultimate one chip" family IC to the TDA8359J, the following waveforms appear on the inputs INA and INB when the components have the values that are shown in the application diagram. The voltage of INA is a bit higher during the flat piece because of the damping resistor compensation that consists of the compensation resistor R_{CMP} and zenerdiode D4.

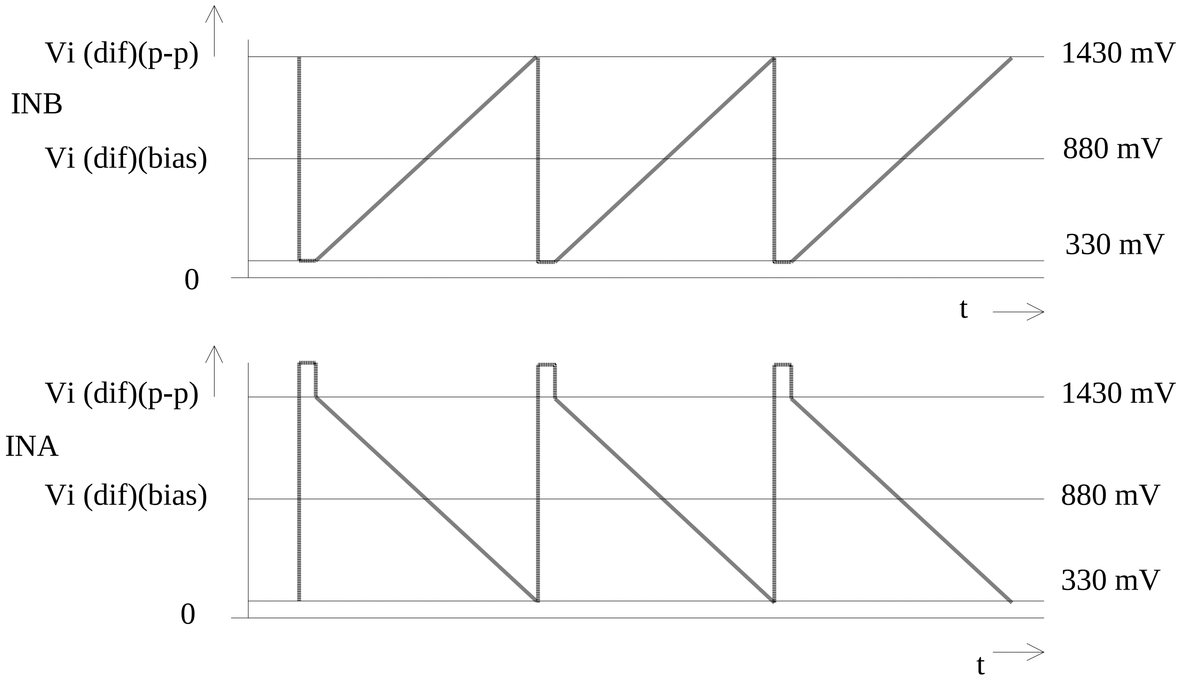


Fig 5: Input voltages of TDA8359J.

The internal input configuration is symmetrical to have a good EMI behaviour, so the external input configuration should also be symmetrical. This means that the drive tracks should be as short as possible and routed next to each other.

The input configuration is as follows:

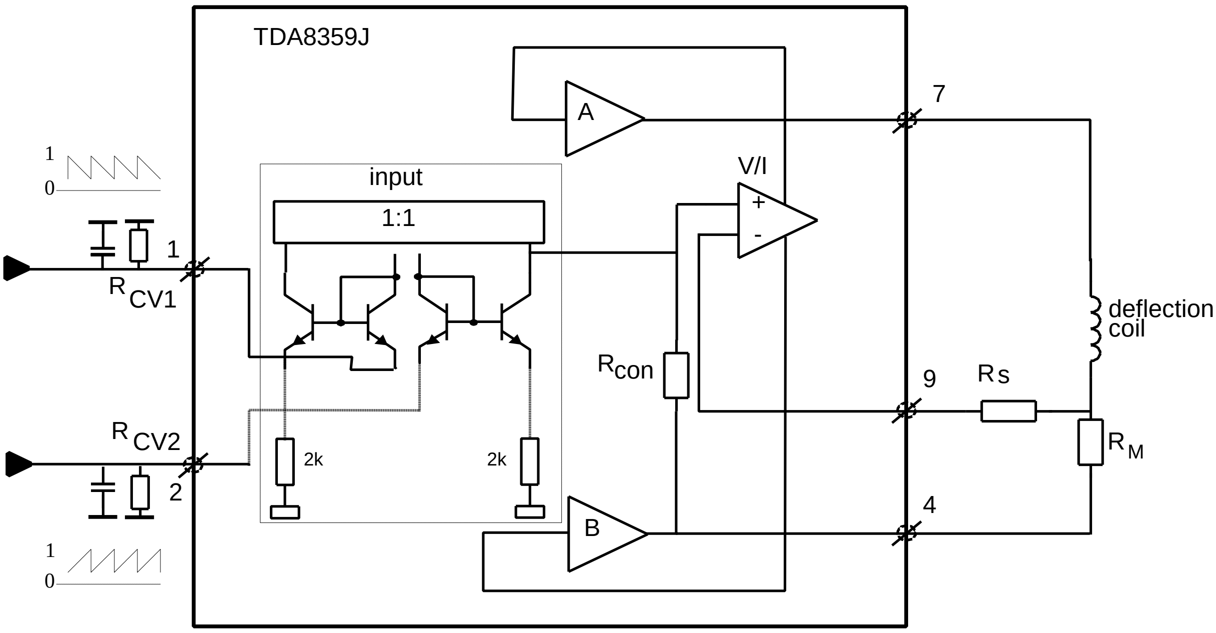


Fig 6: Input configuration.

The relationship between the differential input current and the output current is defined by:

$$2 \times I_{i(dif)(p-p)} \times R_{cv1,2} = I_{coil(pp)} \times R_M$$

So:

$$I_{coil(p-p)} = \frac{2 \times I_{i(dif)(p-p)} \times R_{cv1,2}}{R_M}$$

$I_{i(dif)(p-p)}$ = differential input current (peak-to-peak-value).
$R_{cv1,2}$ = input conversion resistor.
$I_{coil(p-p)}$ = coil current, peak to peak value R_M = measuring resistor.

The actual coil current I_{coil} is approximately 5 to 10 % *lower* than calculated. This depends on the equivalent series resistance which is introduced by connecting the output B pin (4) to the board (soldering quality), the resistance of the printed track (including jumper wire), the connection of resistor R_M and the internal bondwire resistance (typical value of 30mΩ. If the value of R_M is low, the influence of the equivalent series resistance will be high, if the value of R_M is high, then the influence will be less.

With the start of the design it is sometimes difficult to choose component values. Generally a measuring resistor of approx. 10% of the coil resistance will be a good choice.
The next figure gives the vertical drive circuit diagram of a UOC with the vertical output stage TDA8359J.

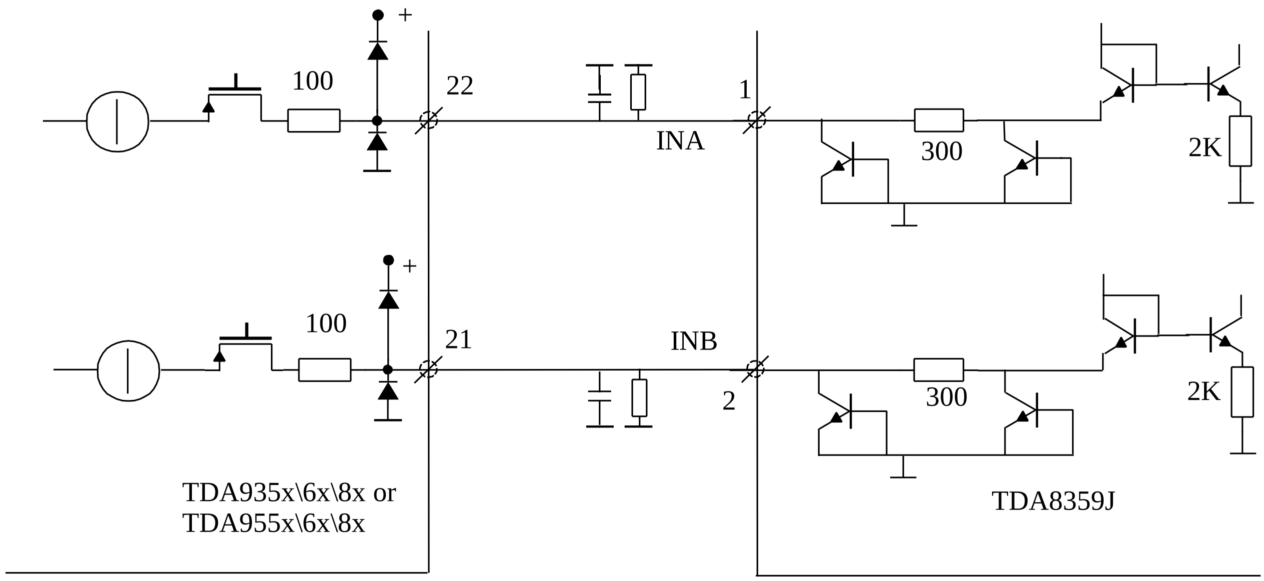


Fig 7: Interconnect between TDA935x\6x\8x or TDA955x\6x\8x and TDA8359J.

2.3.2 Conversion resistors $R_{CV1,2}$ and measuring resistor R_M

The output is adjustable from 0.5 A_{p-p} to 3.2 A_{p-p} mainly by varying and R_M.
The conversion resistors $R_{cv1,2}$ both have the same value and can be calculated by :

$$R_{cv1,2} = \frac{V_{i(dif)(p-p)}}{I_{i(dif)(p-p)}}$$

The value of resistor R_{CV1} and R_{CV2} must be chosen in such a way that $V_{I(bias)} + V_{i(dif)(peak)}$ is smaller than 1500 mV and $V_{I(bias)} - V_{i(dif)(peak)}$ is larger than 300 mV per input pin, for a better linearity.
For the Ultimate One Chip this value is 2kΩ - 2.2kΩ.

The measuring resistor R_M can be calculated by means of the formula:

$$2 \times I_{i(dif)(peak)} \times R_{cv1,2} = I_{coil(p-p)} \times R_M$$

It is advised to choose 1 - 1.4V across R_M.

Example:

We suppose the following:
(according to the application diagram in the specification)

$I_{O(p-p)}$	= 2.4 A_{pp}
$I_{i(dif)(p-p)}$	= 2 x $I_{i(dif)(peak)}$ = 2 x 290µA = 580µA (value is given by vertical driver circuit)
$V_{I(dif)(p-p)}$	= 1.3 V (choose the voltage across $R_{cv1,2}$ between 1Volt and 1.6 Volt)

$$R_{cv1,2} = \frac{V_{i(dif)(p-p)}}{I_{i(dif)(p-p)}} = \frac{1300mV}{580mA} = 2241\Omega$$

E96-value = 2.21kΩ

$$2 \times I_{i(dif)(peak)} \times R_{cv1,2} = I_{coil(p-p)} \times R_M$$

so :

$$R_M = \frac{2 \times I_{i(dif)(peak)} \times R_{cv1,2}}{I_{o(p-p)}} = \frac{2 \times 290mA \times 2241\Omega}{2.4A} = 0.53\Omega$$

E24-value = 0.51Ω

2.4 Feedback Circuit

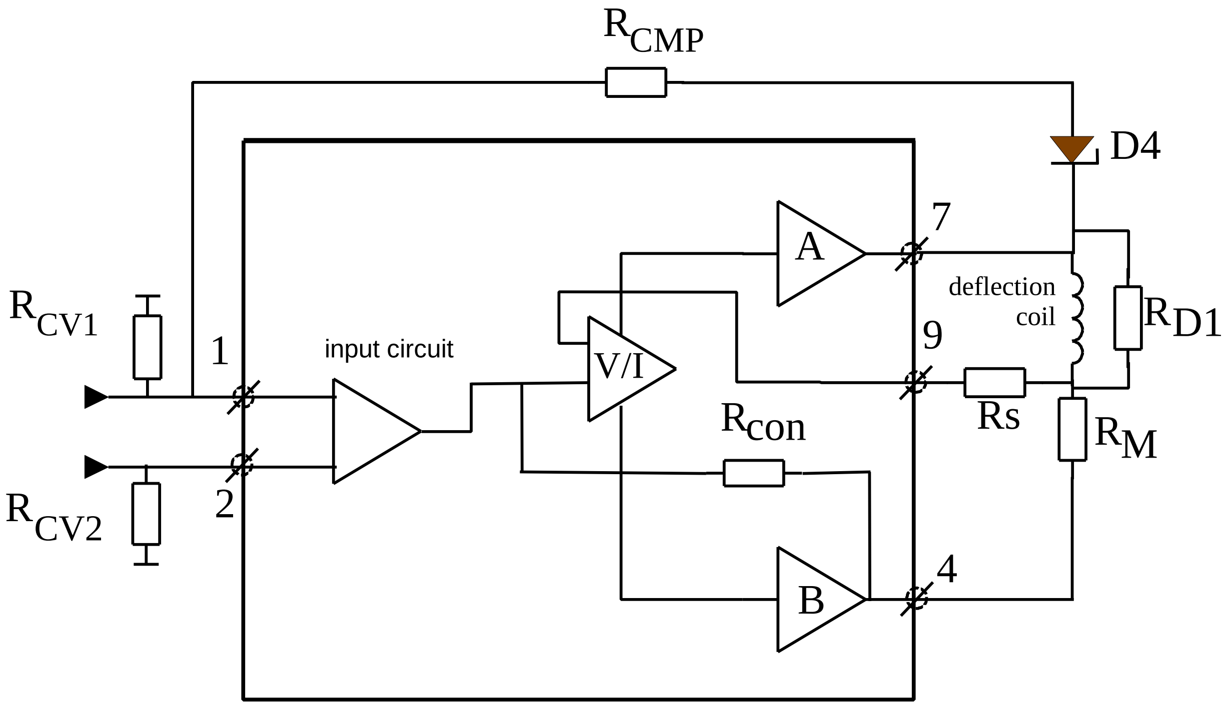


Fig 8: Feedback circuit.

The feedback circuit is build up with a reference between pin 4 (OUTB) and pin 9 (FEEDB), the voltage across R_M and a series resistor R_S (pin 9). This input is connected to a differential V/I converter, which compares the voltage across R_M and the voltage over the internal conversion resistor R_{CON}. If both voltages are not equal the V/I converter drives the output stage until the voltage across R_M is equal to the input voltage.

During flyback, the flyback voltage is put across the deflection coil and the damping resistor R_{D1}. This results in a higher current in the damping resistor and also in the measuring resistor. So the current in the measuring resistor is higher than the intended current in the coil. This affects the moment at which the flyback switch is not conducting anymore. To compensate this, an extra current is added to the current that flows through the conversion resistor R_{CV1}, by means of R_{CMP} and D_4.

2.4.1 Series resistor (R_S)

The purpose of R_S at the Feedback (pin 9) is to prevent oscillations and to achieve equal impedance for the V/I converter, $R_s = R_{con}$ because the V/I converter, see Fig 8 , should see equal input impedance at both inputs. This improves the common mode suppression. The tracks to the inputs are not the same. One track is connected internally to resistor R_{CON}. The other input has an external wire. To match R_{CON}, the series resistor R_S is connected between the deflection coil and pin 9. Choose R_S about 2.7kΩ.
If the output waveform should contain some oscillations, the value of R_S should be slightly changed. A small capacitor of 1pF-100pF between pin 9 (FEEDB) and pin 4 (OUTB) could also help for minor oscillations.

2.5 Vertical output stage

The Philips TDA8359J vertical output stage uses a class G bridge concept. (see Fig 9).
The class G concept allows a very efficient DC coupling of the vertical output stages. This matches perfectly with modern driving circuits, circuits which can change settings like amplitude, shift and start scan, that are controlled via the I^2C bus.
The deflection coil in series with resistor R_M is connected between the two outputs pin 7 and pin 4. Resistor R_M is used to measure the current through the coil. The voltage across resistor R_M is the input voltage for the feedback stage.

The two output amplifier stages A and B are nearly identical. Output stage top MOSFET A (M2) and bottom MOSFET B (M3) and diode D3, conduct for the first part of the sawtooth (coil) current and are supplied from the main supply (V_P). Output stage top MOSFET B (M1) and bottom MOSFET A (M4) conduct for the second part of the sawtooth current and is supplied via the same main supply voltage.

MOSFET (M5) is the flyback switch. It is supplied through a higher supply voltage (V_{FB}) than the main supply voltage to achieve a short flyback time.
The maximum allowed value of the main supply voltage is 18 Volt and for the flyback supply voltage 66 Volt.

To prevent a short circuit between the main supply and the flyback supply, a diode (D1) is placed in series with the top MOSFET A (M2) of the output stage. To prevent conduction of the parasitic diode of the flyback switch (M5), (during the first part of the flyback period) a diode (D3) is placed in series with it.

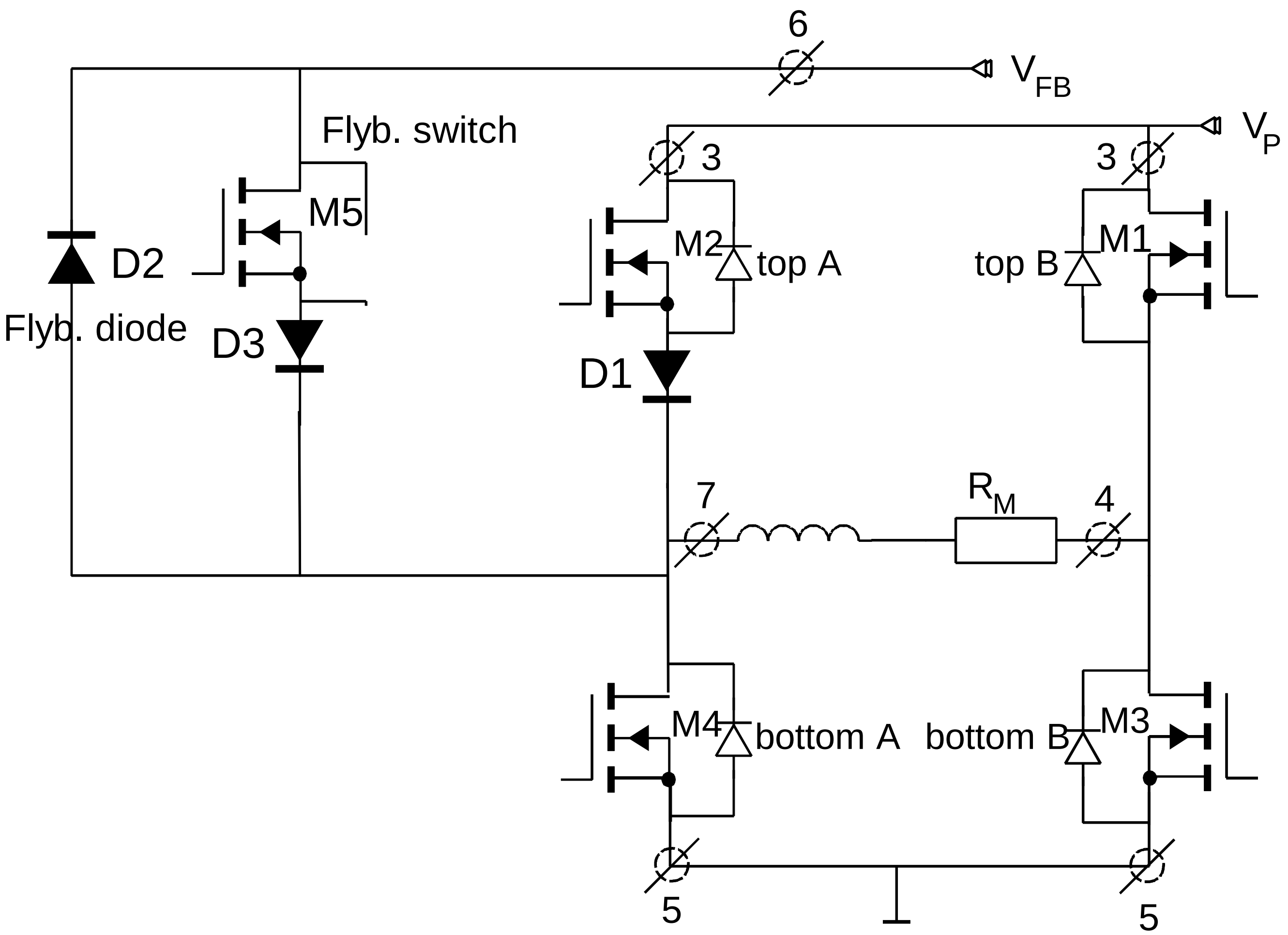


Fig 9: Output configuration TDA8359J.

The current flow through the output MOSFETs and the vertical deflection coil can be considered in four different parts/stages: the first part of the vertical scan, the second part of the vertical scan, the first part of the flyback and the second part of the flyback. The first and second part of the vertical scan will be discussed in the following section, while the flyback part will be explained in the next paragraph (2.6)

The current path in the vertical output bridge for the first part of the scan is illustrated by the dotted line in Fig 10.
In this figure one can see that the current flows from the main supply pin via top MOSFET A (M2) and diode (D1) of output A in the vertical deflection coil and measuring resistor R_M , via bottom MOSFET B (M3) of output B to ground. The current path for the second part of the scan is illustrated by the dotted line in Fig 11.

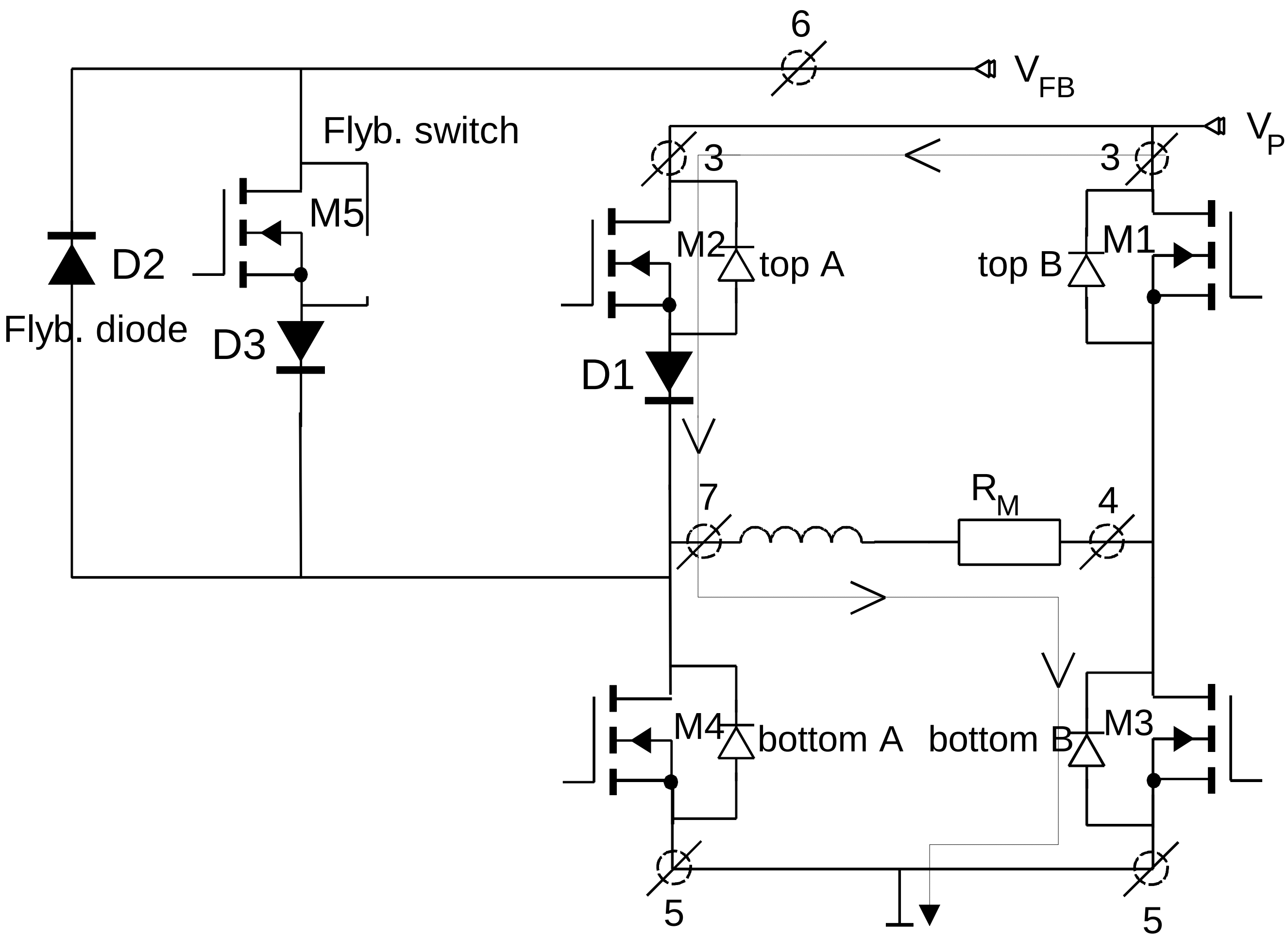


Fig 10: Current path, first part of scan.

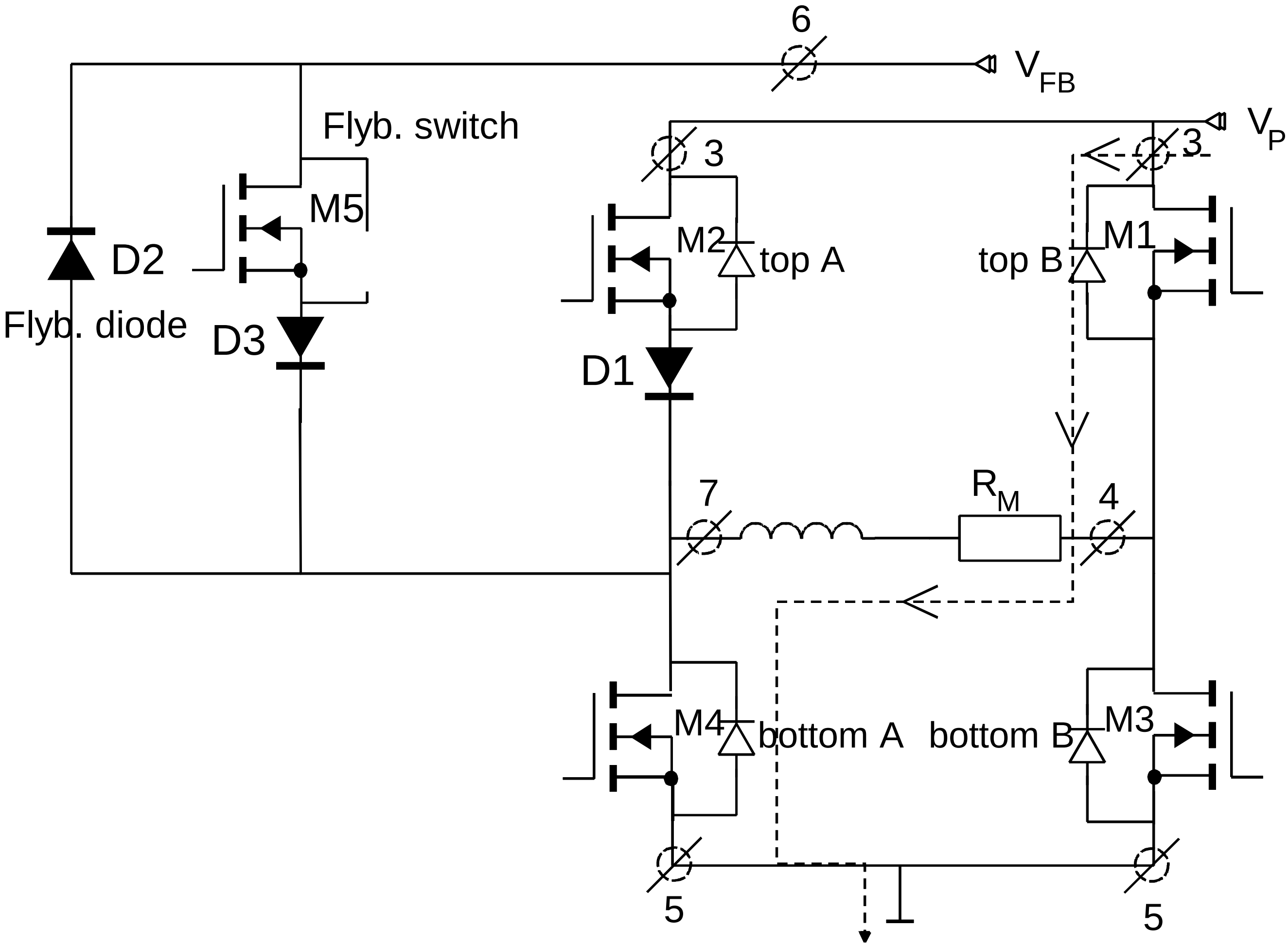


Fig 11: Current path, second part of scan.

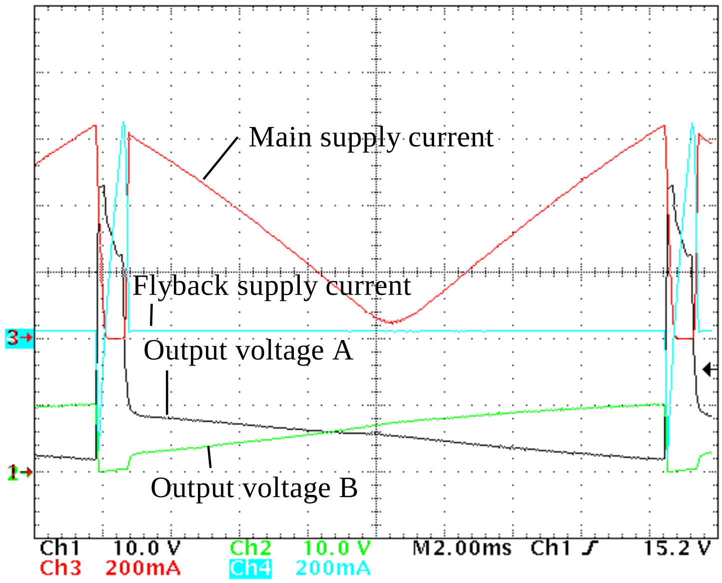
During the second part of the scan time, the current flows from the main supply pin via top MOSFET B (M1) via output B in the measuring resistor R_M and the vertical deflection coil, via bottom MOSFET A (M4) of output A to ground. During the scan time, the current that flows through the deflection coil has a sawtooth shape and the main supply (V_P) supplies the current that is needed.

The supply current will be at it's maximum at the start of the scan, decreasing to the middle of the scan and than increasing until the end of the scan.

In Fig 12 waveforms during scan are shown, these pictures are made with a digital oscilloscope. In this figure it is seen that the lines of output voltages A and B contain a small jump, when switching from the first part of the scan to the second part of the scan. This is because diode D1 causes a voltage drop. This is not crossover. The line of the coil current is linear.

Furthermore one can see that the lines of the Output A voltage and the Output B voltage do not cross in the middle of the scan time. This is because the voltage drop across the deflection coil, for the first part of the scan is different than the voltage drop across the deflection coil during the second part of the scan. This is caused by the coil impedance which exists of a resistive part and an inductive part. So the total voltage drop across the deflection coil exists of a resistive voltage and an inductive voltage. For the first part of the scan the inductive contribution and the resistive contribution are of opposite sign, while for the second part of the scan the inductive contribution and the resistive contribution have the same sign. See also paragraph 2.10.1.

So, if the deflection coil has a *relatively large* L (selfinduction), the voltage drop during the *first part* of the scan has a *lower value* compared to the value of the second part of the scan.
That's why the crossing point of the lines of output A and output B shift to the left, when the L of the deflection coil increases.



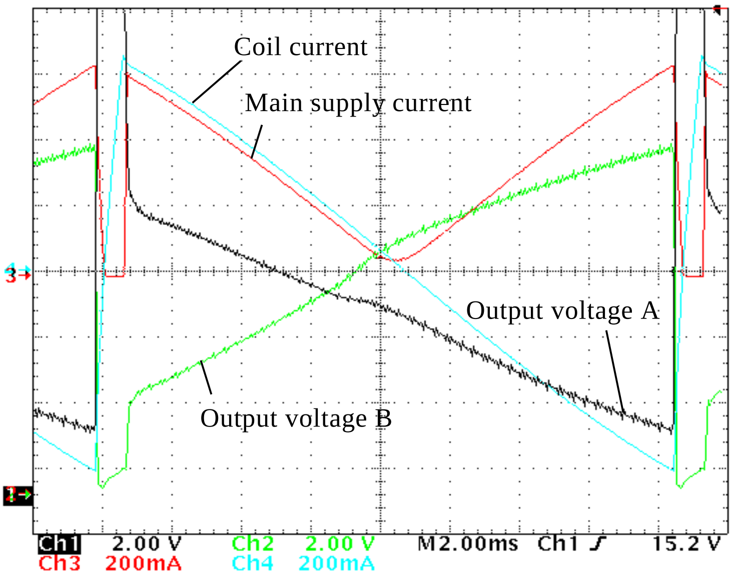


Fig 12: Waveforms during scan.

2.6 The flyback switch

In the TDA8359J concept the value of the supply voltage (V_P) and the flyback supply voltage (V_{FB}) can be chosen independently. In general, the flyback supply voltage will be chosen much higher than the supply voltage that is needed for the scan. A ratio of 2 to 4 is possible, with a maximum of 66 Volt. This is much higher than the value that is reached in conventional designs with a flyback voltage generator circuit (in general a ratio of 2, maximum). The flyback supply voltage is almost fully available at the output pin of stage A, thus across the deflection coil.

At the end of the scan time the input drive voltage will change fast in direction. The coil will try to maintain the present current level. At this moment the output signal cannot follow the input signal, which forces the amplifier into an open-loop condition. The flyback pulse will start.

The flyback can be divided in part A and B, see Fig 13. Due to the high voltage across the coil, the first part A has a short duration. Part A ends when the current in the deflection coil becomes zero.

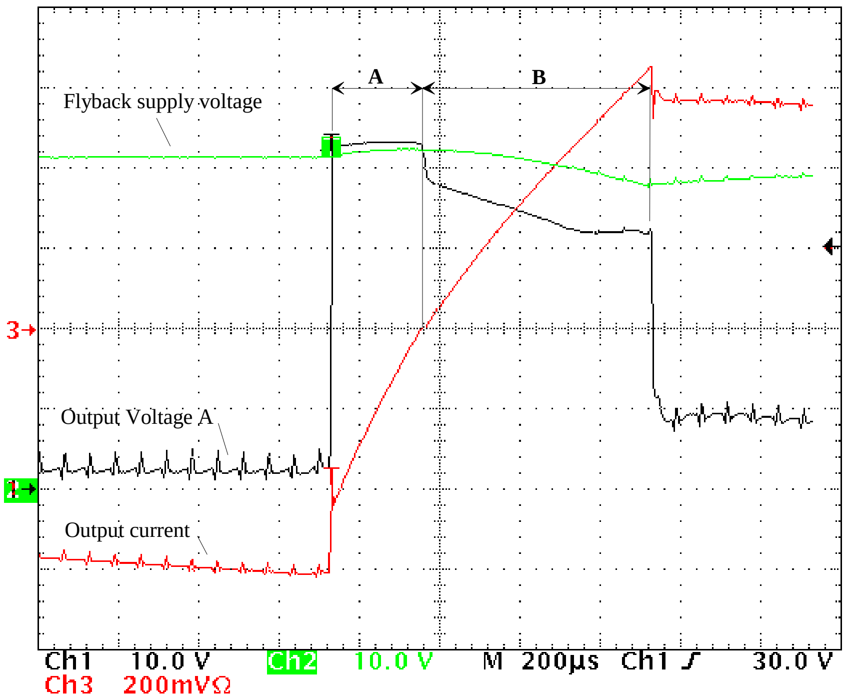


Fig 13: Waveforms during flyback.

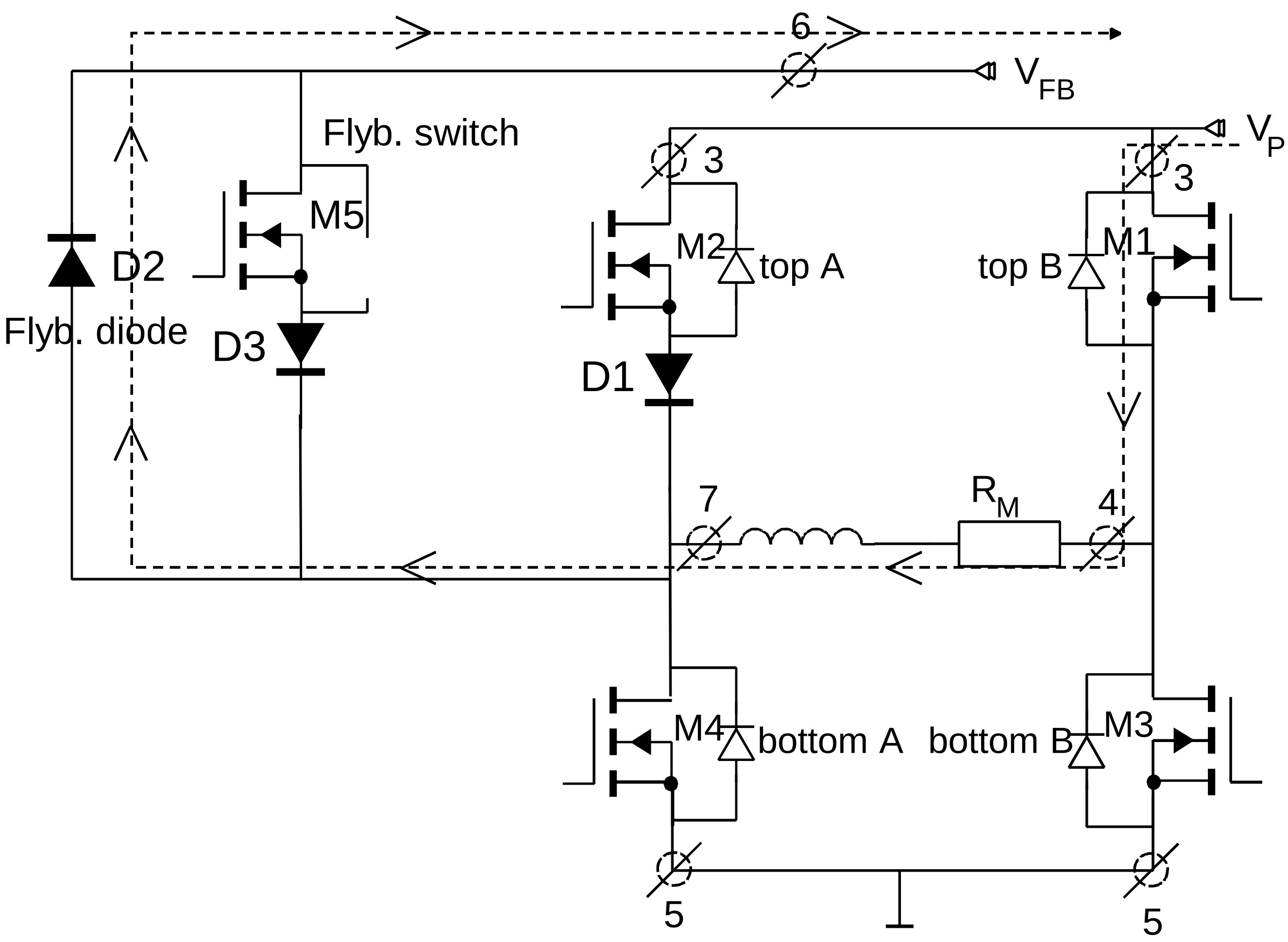


Fig 14: Current path, first part of flyback.

At the start of the first part of the vertical flyback the internal drive signal switches off the top MOSFET of stage B (M1). The current in the deflection coil seeks a way out and the voltage at the output pin 7 increases and so the voltage at pin 4 will drop and tries to go below zero. Now, a clamp circuit is activated to keep this voltage above zero, due to this clamp, only the top MOSFET of stage B (M1) will conduct, otherwise the parasitic diode across bottom MOSFET M3 would conduct which could cause substrate-currents which could cause a malfunction of the device.
The voltage at the output (pin 7) increases and the flyback diode D2 conducts. This output voltage becomes about 2 Volt higher than the flyback supply voltage (=voltage across diode D2), see Fig 13. The current is fed into the flyback supply capacitor.
The current goes now through the top MOSFET of stage B (M1), the external measuring resistor R_M, the deflection coil and the internal flyback diode (D2) into the flyback supply, see the dotted line in Fig 14.

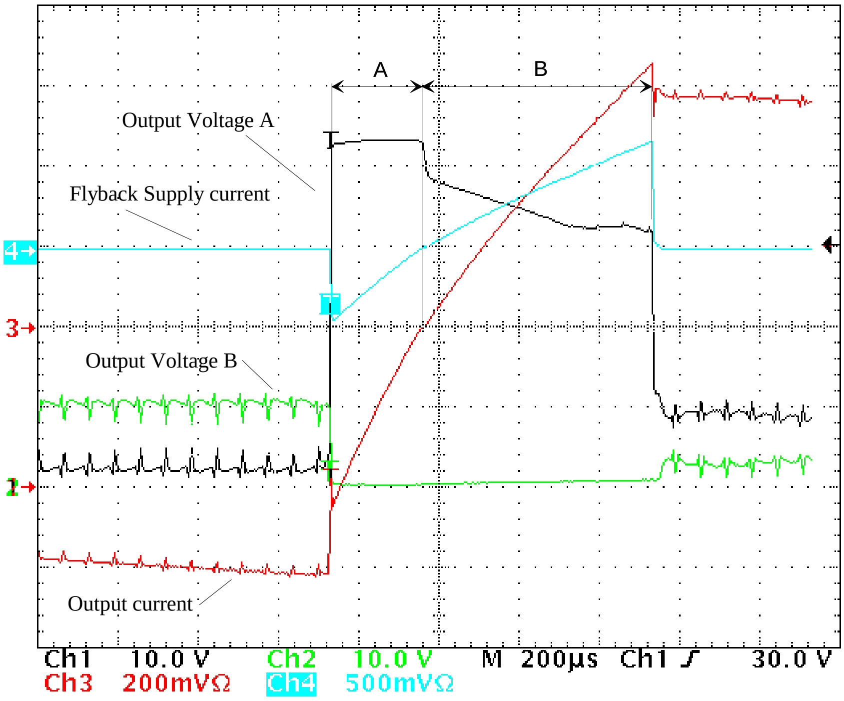


Fig 15: Waveforms during flyback, including supply flyback current.

The current flow for the second part “B” of the vertical flyback is given below.

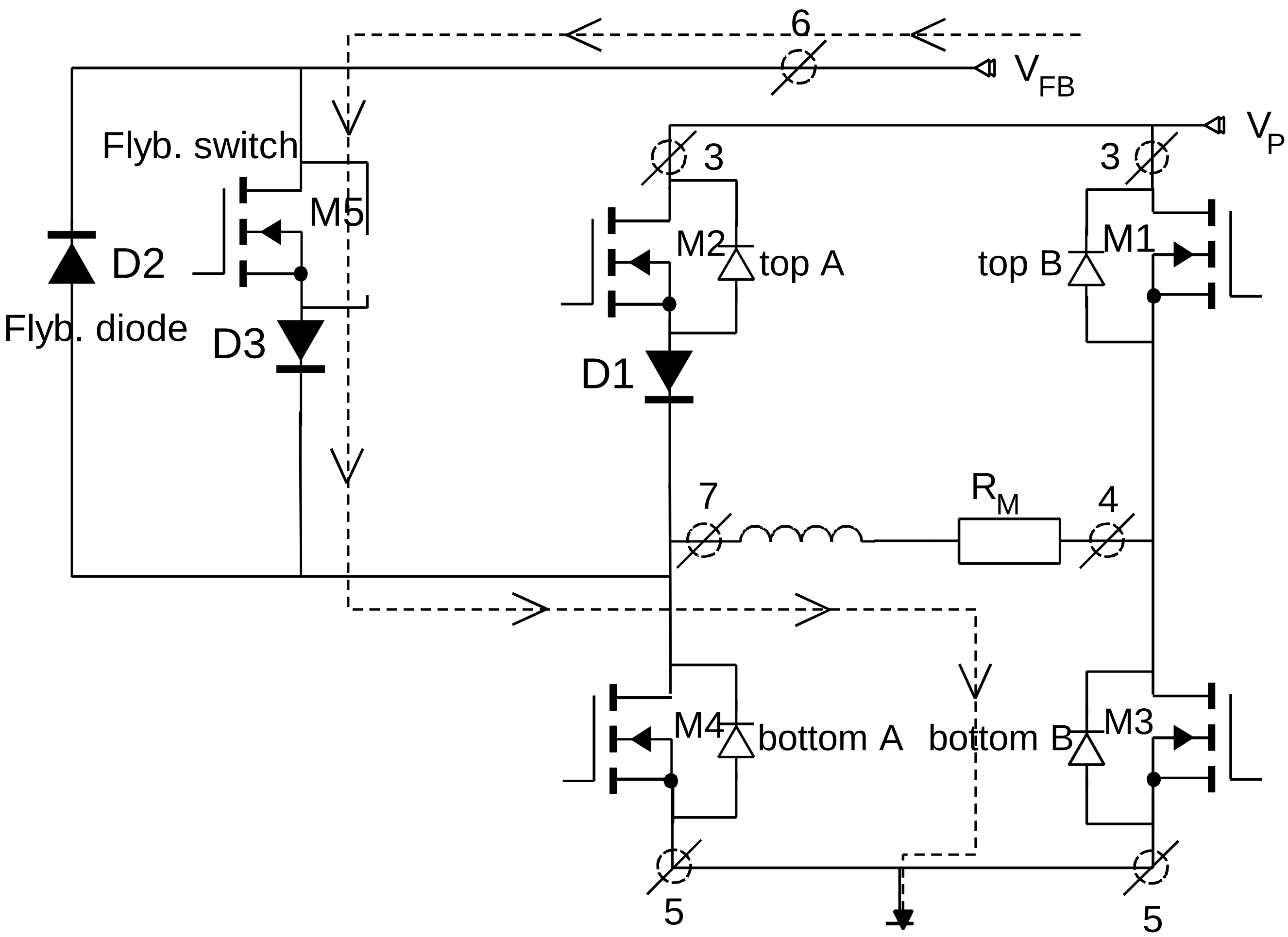


Fig 16: Current path, second part of flyback.

The second part, part B of the flyback pulse, starts when the current in the deflection coil crosses the zero level, see Fig 15. Now, the current in the deflection coil is supplied by the flyback voltage supply and the flyback switch (M5) conducts. The current flows via the flyback switch (M5), the internal diode (D3), the deflection coil, the measuring resistor R_M ,via the bottom MOSFET of stage B (M3) to ground, see Fig 16.
(Due to a voltage loss across the flyback switch (M5) + the internal diode (D3), the output voltage at pin 7 is about 7.5 Volt to 9 Volt lower than the flyback supply voltage, see Fig 13. This voltage drop depends on the current in the coil, a higher current means a higher loss and thus a higher voltage drop {for details, see specification}).

The current through the coil will become positive now and will increase until it reaches a certain value, which is proportional to the level of the input signal. Then the feedback loop is closed and the flyback switch is switched off. The scan sequence can start again.

The waveform during part B of the output A voltage has a shape that is created by the adaptive control of the flyback switch which operates as following : the output current of the flyback switch is measured on a certain level onwards, the drive of the flyback switch is increased, thus lowering the impedance of the flyback switch and also lowering the output A voltage, untill it has reached a certain stable value. Now the end of the flyback is reached.

2.7 Damping resistor R_{D1}

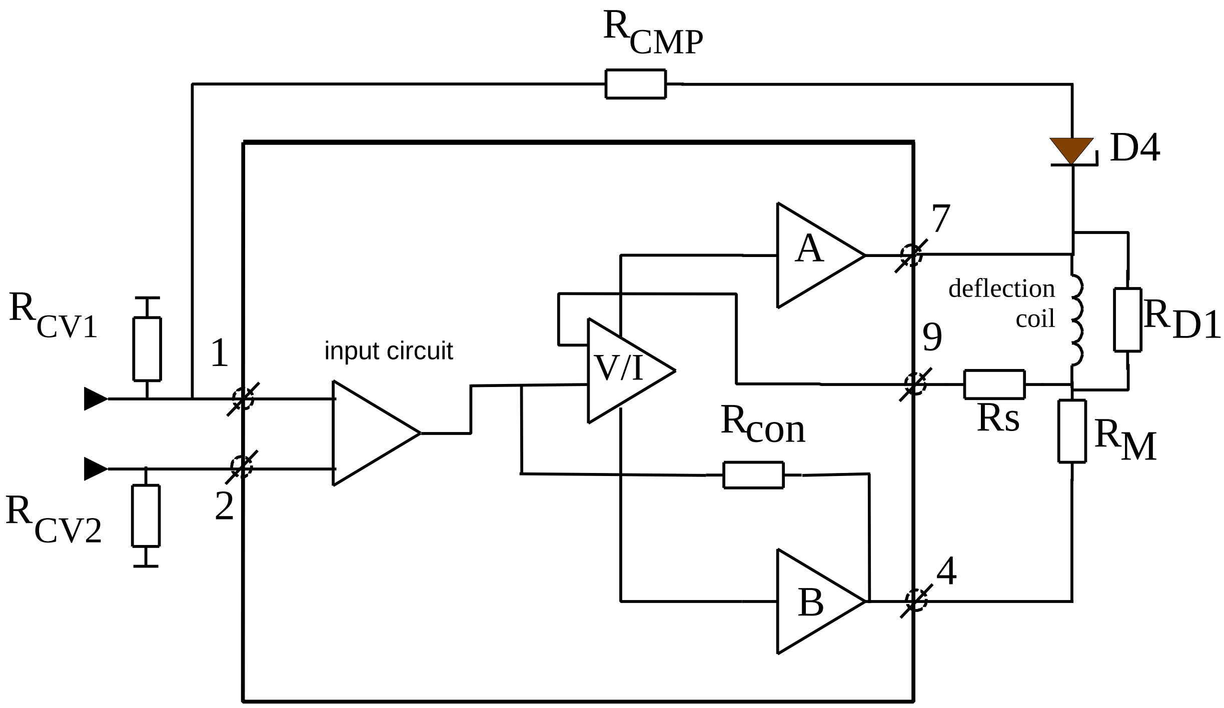


Fig 17: Damping resistor compensation.

A damping resistor R_{D1} is connected across the deflection coil for loop stability. The value of R_{D1} depends on the deflection coil and it should be as high as possible.
Choose R_{D1} about 270Ω - 300 Ω. If there is already a resistor mounted on the deflection coil assembly on the picture tube, another resistorvalue is possible.

note :
If the damping resistor is situated on the deflection coil assembly, the following picture is seen by measuring the current *through the wires from PCB to the coil connector*. A current increase of about 200mA. This is the current through the damping resistor on the deflection coil assembly.

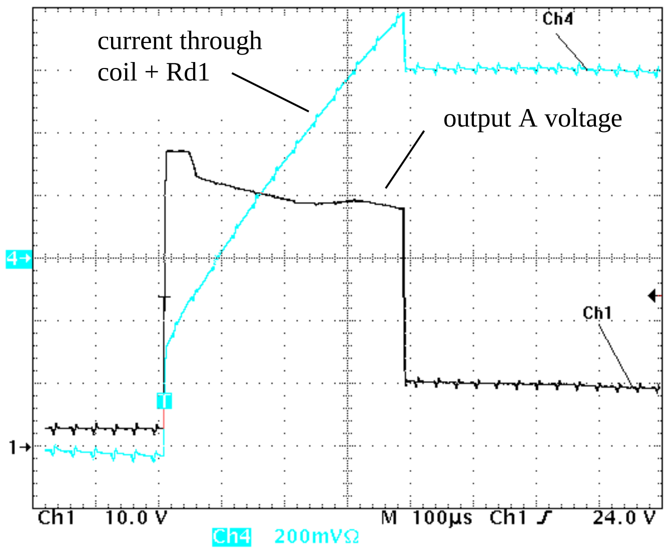


Fig 18: Current through deflection coil + R_{D1}.

The current through the damping resistor R_{D1} is high during flyback compared to the current during scan time.
The damping resistor current is added to the deflection coil current via the measuring resistor R_M. Without precautions this results in a too low current in the deflection coil at the start of the scan.
This current can be compensated to achieve a short settling time, by means of an external circuit. This circuit consists of a resistor (R_{CMP}) in series with a zenerdiode (D4) and is connected between the input INA (pin1) and the output OUTA (pin7).
During flyback, if the output voltage becomes higher than the value of the zenerdiode D_4 (V_Z), a current will flow into the external circuit (R_{CMP} + D_4) and will be added to the input stage. The value of the current is determined by resistor R_{CMP} and the value of the zenerdiode D_4. This current compensates the effect of the current in the damping resistor during flyback.

2.8 Protection Circuits

The TDA8359J has protection circuits for:

- Too high crystal temperature.
- Over-voltage of output stage A.

2.8.1 High crystal temperature

A temperature sensor is located on the die of the TDA8359J. If this sensor detects a temperature of approximately 170 °C, the protection circuit activates. The protection circuit reduces the drive of the output stage and the current through the coil is reduced. The guard output becomes high and can be used to signal the microprocessor that a fault condition occured.

2.8.2 Over-voltage output A

The over-voltage protection is activated, when the voltage of output stage A (pin 7) increases above 68 Volt, which can occur during voltage peaks (spikes). During these conditions, the protection circuit switches on MOSFET (M4) of output stage A, so M4 conducts and the output voltage at pin 7 decreases. See Fig 9: Output configuration TDA8359J.

To prevent a short-circuit of the vertical flyback voltage at pin 9, at active over-voltage protection, the flyback switch M5 is not conducting.

Output stage B is ‘self-protecting’ because if an overvoltage occurs at output stage B (pin 4), the parasitic diode from the top MOSFET (M1), conducts and the current is led to the elco at pin 3. (This is not possible at output stage A, because diode D1 would block the current path to the elco at pin 3)

2.9 Guard Circuit

The guard output signal generates a pulse during every vertical retrace and at other conditions when the picture tube should be blanked. It can also be used to prevent the picture tube from burn-in, (due to faulty vertical deflection conditions) and as a vertical synchronisation signal to a microprocessor for e.g. On Screen Display.
This guard pulse can be monitored by the deflection controller, such as the Ultimate One Chip.

The guard output is active (high) for one of the following conditions:

a) during the flyback (retrace) period.
b) during an open-loop condition.
c) during thermal protection ($T_J \approx 170°C$).

An open-loop situation occurs when the output current is clipping.
The output of the guard circuit is a current source, which can deliver an active current of minimal 1 mA, at a voltage of 4.5 Volt.

The guard output can be monitored by the Ultimate One Chip family or other driver circuits. In the first case the vertical deflection works correctly when the guard pulse:

1) is > 3.65Volts
2) has a duration > 30µseconds when active
3) becomes < 3.65Volt before the measuring lines of the UOC, otherwise *discoloration could appear*

During scan (in case of the Ultimate One Chip), the DC level of the vertical guard pulse is not critical but it should be below the 3.65V detection level.
Any other waveform is considered as a ‘vertical guard failure’ which will lead to blanking of the RGB outputs, see Fig 19.

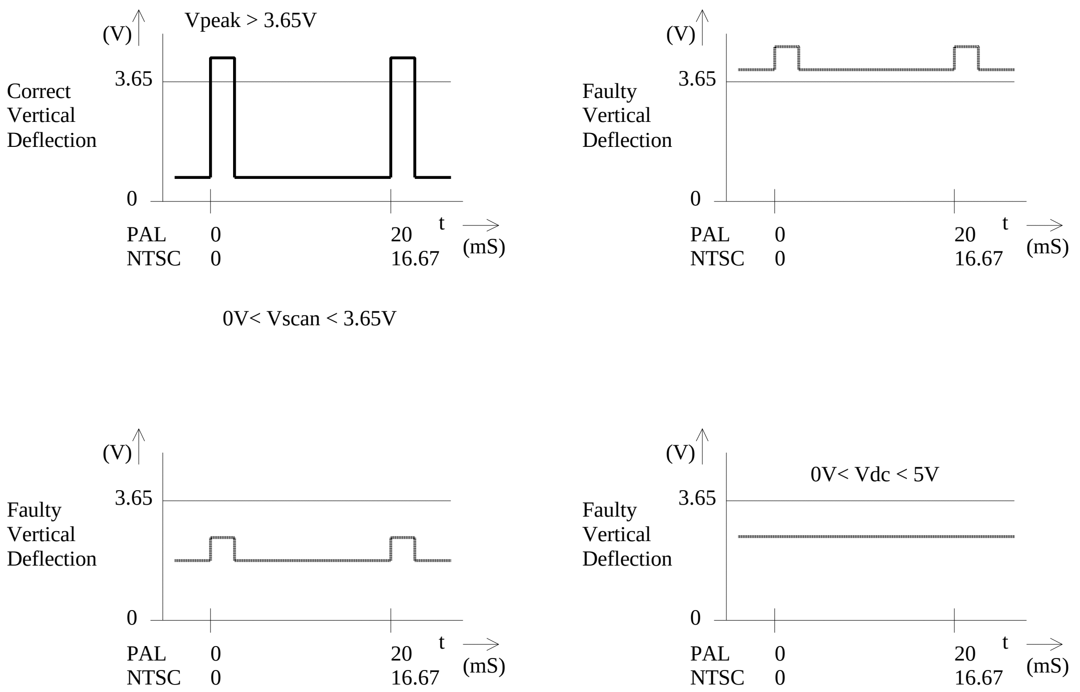


Fig 19: Guard pulse with TDA884x\5x and TDA 935x\6x\8x N1.

2.9.1 Guard pulse connection

The next figure shows an application diagram that combines the two beam current limiting functions (PWL and ABL) of a One Chip family device with the vertical guard function of the TDA8359J.

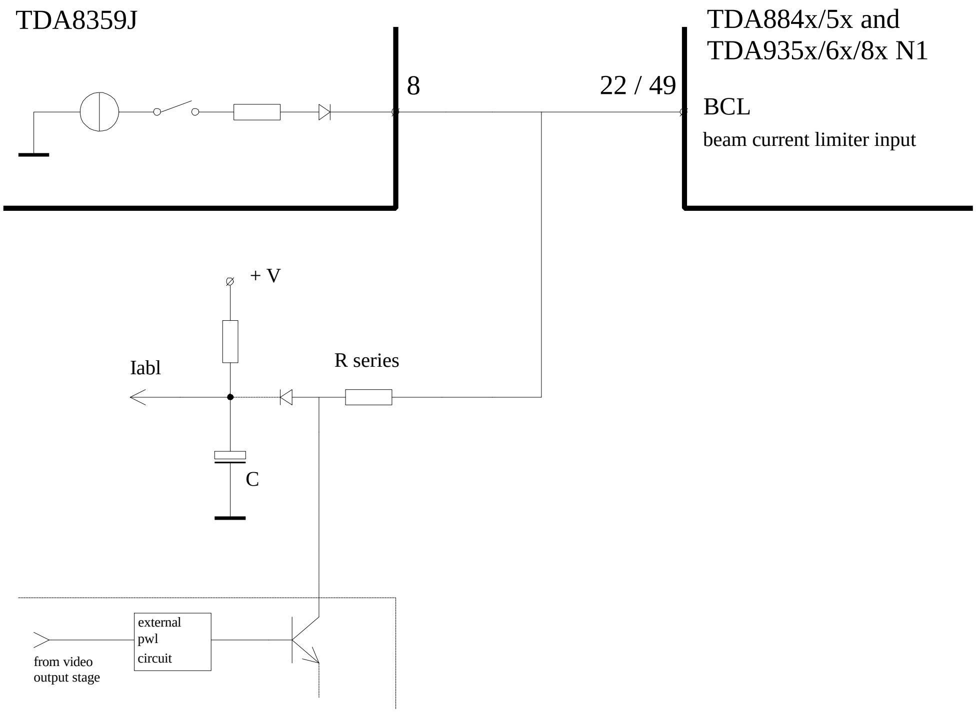


Fig 20: Guard application PWL and ABL.

The combined input of the TDA884x\5x and the TDA935x\6x\8x N1 family has the following characteristics:

- If the BCL is not active, the voltage on pin 22 is 3.3 Volt, or higher.
- If BCL is active the internal impedance of pin 22 is 40 kOhm.
- The current that has to be pulled out of the BCL-pin is constant (approximately 40µA) over the whole range.

The diode in series has two functions:

- Prevent that the voltage at pin 22 can be driven above 3.65 Volts that can disturb the vertical guard function.
- Isolate pin 22 from capacitor C in order to ensure a fast PWL function of the TDA884x\5x and the TDA935x\6x\8x N1 family.

Important to know is that the BCL-circuit forms a load to the output signal of the vertical guard output circuit. This load should be below 1mA (at 3.65V pulse level). The minimal series resistor at pin 22 can be calculated by:

$$R_{series} = \frac{V_{guard} - V_{c\,\min} - V_{fdiode}}{I_{guard\,\max}} = \frac{3.65V - 0V - 0.65V}{1mA} = 3k\Omega \qquad V_{fdiode} \approx 0.65V$$

In this formula only the minimum voltage on the averaging capacitor is determined by the design of the ABL-function. (The minimum voltage on the averaging capacitor occurs at maximum beam current.). In case $V_{Cmin} = 0$ V; $R_{series} = 3$ kΩ. It is wise to use a higher value as series resistor, such as 5.6 kΩ.
Take also into consideration that in some applications V_{Cmin} can become negative.

2.9.2 Guard with TDA935x\6x\8x N2 and TDA955x\6x\8x as driver circuit

In the TDA935X/6X/8X N2 and TDA955X/6X/8X family the vertical guard function has been combined with the black current measuring input. For a reliable operation of the protection system and to avoid that the black current stabilisation is disturbed, the end of the guard pulse should not overlap the RGB measuring pulses. Therefore this pulse must end before the start of the black current measurement lines.
If the flyback time is too long or an open loop situation appears, the guard pulse is not ended before the black current measurement line and the black current stabilisation is disturbed.

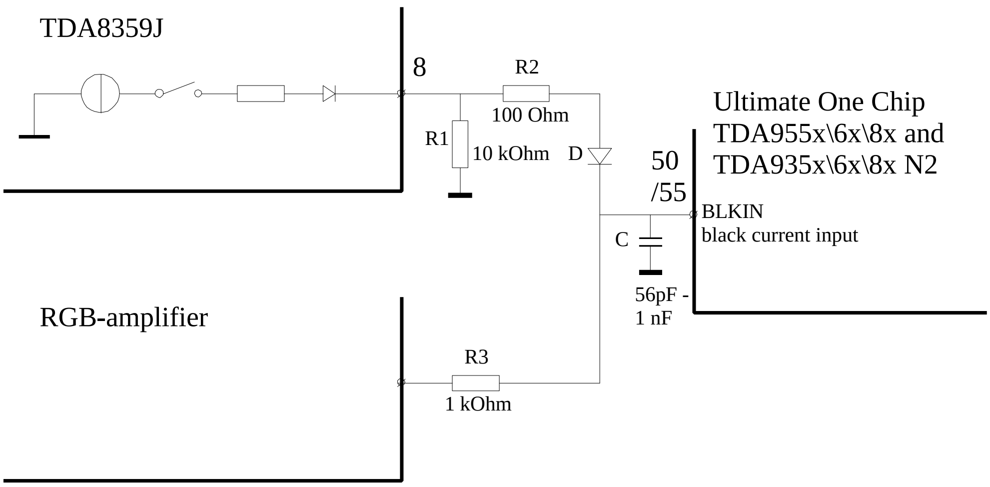
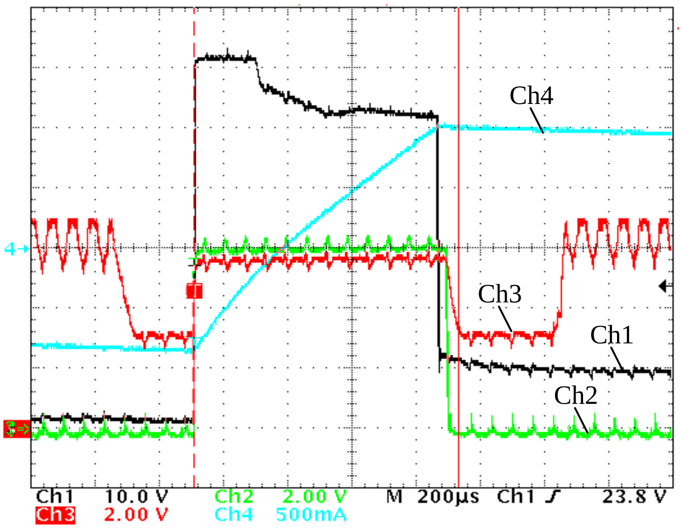


Fig 21: Guard connection with TDA935x/6x/8x N2 and TDA955x\6x\8x

In Fig 21 one can see the application diagram for connecting the guard to the TDA955X/6X/8X and TDA935X/6X/8X N2 family. The GUARD pin of the TDA8359J is connected to pin 50/55 BLKIN of the TDA955X/6X/8X and TDA935X/6X/8X N2 family. The black-current measurement output of the RGB-amplifier is also connected to pin 50/55 BLKIN of the TDA955X/6X/8X and TDA935X/6X/8X N2 family.

The output stage of the guard in the TDA8359J is a current source, so the resistor R1 of 10 kΩ is used to have a quicker fall time of the guard pulse. The capacitor C (56pF – 1nF) is used to reduce possible disturbance. Diode D can be used for protection.

In **Error! Reference source not found.** are scope picture of an application, which uses the guard function. In this application the diode D is used. The TDA9567H is used as driver circuit.



Ch1 = Voltage pin 7 OUTA of TDA8359J
Ch2 = Voltage pin I_{om} of RGB-amplifier
Ch3 = Voltage pin 8 GUARD of TDA8359J
Ch4 = Current pin 7 OUTA of TDA8359J

Fig 22: Scope picture of application with guard.

2.9.3 Guard pulse connection with high load

If the vertical guard pulse, besides the guard-function, is also used as V-sync, care must be taken to prevent that the maximum load is exceeded. In this case it's better to buffer the vertical guard output signal by means of a PNP-emitter follower. In order to separate the BCL-voltage on pin 22 / 49 from the buffered vertical guard (V-sync) signal, a diode from the emitter of the PNP to BCL-pin should be added, otherwise the vertical guard signal that is used as V-sync information will be disturbed. See Fig 23.

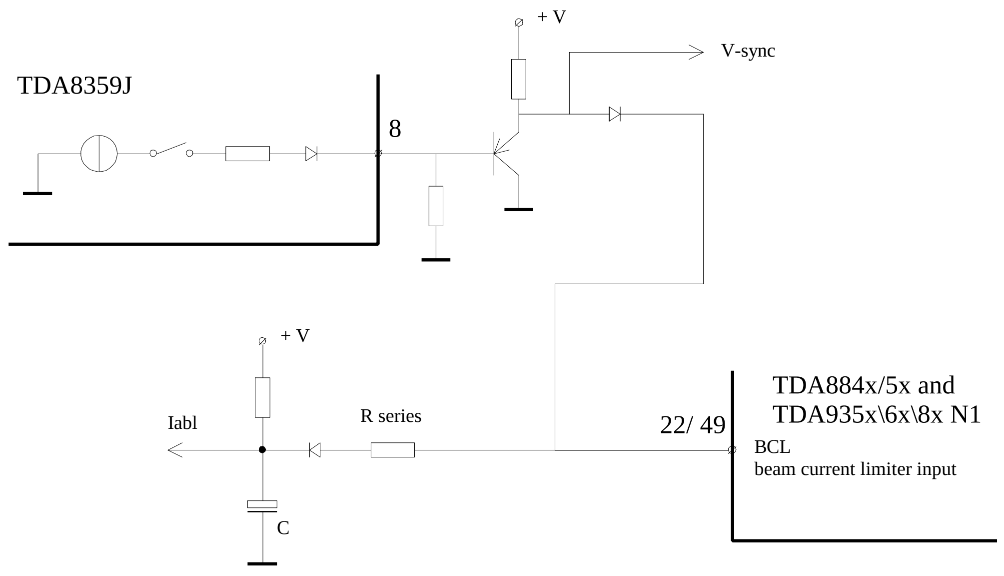


Fig 23: Application for guard pulse with high load.

2.10 Supplies

The TDA8359J concept has two power-supplies, a flyback supply and a main supply which are calculated independently. The principle of operating with two supply voltages (class G) allows the use of an optimum main supply voltage V_P for scan and an optimum flyback supply voltage V_{FB} for flyback. This method achieves very high efficiency.

2.10.1 Calculation of the main supply

To calculate the minimum required supply voltage, several specific application parameters have to be known. These parameters are the required maximum (peak) deflection coil current, the coil-resistance, the coil-inductance and the measuring resistor. The maximum coil peak current should also include overscan.
The deflection coil resistance should be multiplied by 1.2 in order to take account of hot conditions.

The output voltage cannot become as high as the supply voltage nor as low as the ground, this is called voltage loss and should be taken in account when calculating the supply voltage. According the specification, the voltage losses $V_{loss(1)}$, $V_{loss(2)}$ are the sum of voltages across the transistors in the internal current paths at a temperature of Tj ≈ 125 °C.
For the first part of the scan : $V_{loss(1)} = (V_p\text{-}V_{outA}) + (V_{outB}\text{-Gnd})$ and for the second part of the scan $V_{loss(2)} = (V_p\text{-}V_{outB}) + (V_{outA}\text{-Gnd})$.
For the TDA8359J, $V_{loss(1)}$ = 6.6V maximum and $V_{loss(2)}$ = 4.8V maximum at I_o = 1.6A peak. The voltage loss as a function of the output (peak) current is given in Fig 24. The values in this figure specify the sum of the voltage losses at T_J ≈ 125 °C.
The temperature coefficients for $V_{loss(1),(2)}$ are positive values.
$V_{loss(1)}$ is higher than $V_{loss(2)}$ because of the extra voltage drop across the internal diode D2, see Fig 9.

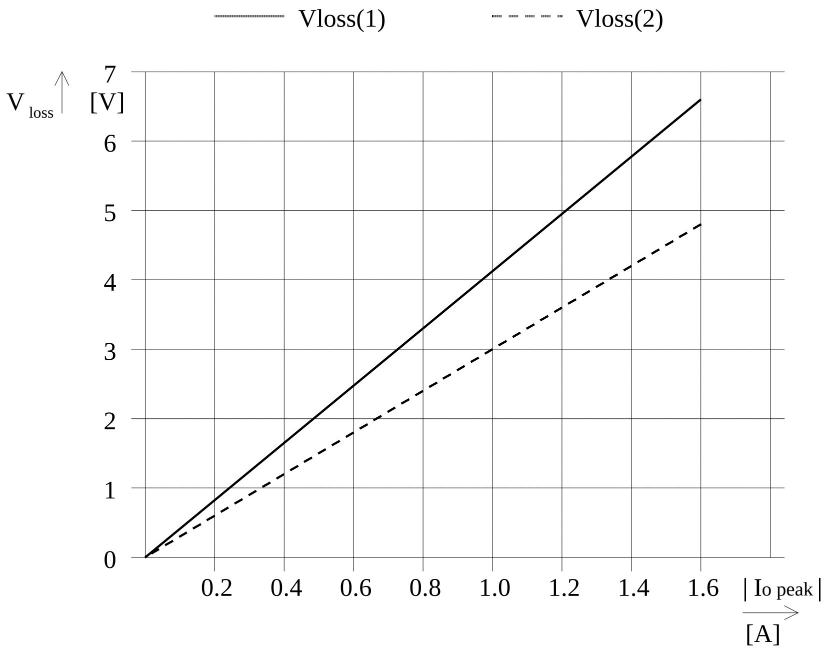


Fig 24: Voltage loss of the output stage.

There is a voltage drop across the coil during scan which is determined by the coil impedance. The coil impedance exists of a resistive part and an inductive part so the total voltage drop across the coil exists of a resistive voltage and an inductive voltage. For the first part of the scan the inductive contribution and the resistive contribution are of opposite sign, while for the second part of the scan the inductive contribution and the resistive contribution have the same sign.

The required power supply voltage V_P for the first part of the scan:

$$V_{P(1)} = I_{coil(peak)} \times (R_{coil(hot)} + R_M) - L_{coil} \times 2 \times I_{coil(peak)} \times f_{vert(\max)} + V_{loss(1)}$$

The required power supply voltage V_P for the second part of the scan :

$$V_{P(2)} = I_{coil(peak)} \times (R_{coil(hot)} + R_M) + L_{coil} \times 2 \times I_{coil(peak)} \times f_{vert(\max)} + V_{loss(2)}$$

$I_{coil(peak)}$ = maximum coil (peak) current

$R_{coil(hot)}$ = $R_{coil(cold)}$ * 1.2 (for hot conditions at 70 °C)
R_M = measuring resistor
L_{coil} = induction of the coil
$f_{vert(max)}$ = maximum vertical frequency
$V_{loss(1),(2)}$ = internal voltage losses

Eventually, after calculating the voltage supply by means of the above formulae, the minimum required value has to be the highest of the two values $V_{P(1)}$ and $V_{P(2)}$. Eventually, this value has to be increased by 5% to 10 % due to spread in the line output transformer and the deflection coil.

In the next example is shown how the main supply is calculated:
We suppose the following:

$|I_{coil(peak)}|$ ≈ $|I_{o(peak)}|$ = 1.2A (the current in the damping resistor R_D can be neglected if R_D is not too low)
R_{coil} = 6 Ω * 1.2 = 7.2 Ω
R_M = 0.5 Ω
L_{coil} = 5 mH
$f_{vert(max)}$ = 50 Hz
$V_{loss(1)}$ = 4.9 V (see Fig 24)
$V_{loss(2)}$ = 3.6 V (see Fig 24)

First part of scan:

$$V_{P(1)} = 1.2 \times (7.2 + 0.5) - 5 \times 10^{-3} \times 2 \times 1.2 \times 50 + 4.9 = 13.54V$$

Second part of scan:

$$V_{P(2)} = 1.2 \times (7.2 + 0.5) + 5 \times 10^{-3} \times 2 \times 1.2 \times 50 + 3.6 = 13.44V$$

So we must choose 13.54 V and increase this value by 5% to get the minimum required supply voltage, V_P = 14.2V.

2.10.2 Calculation of the flyback supply

The flyback time is basically set by the value of the flyback voltage. So the flyback time can be optimized by choosing the appropriate flyback voltage. At the end of the flyback time, a settling time is needed at the start of the scan before the linear scan begins. Generally the settling time is covered by the overscan time. For the TDA8359J the settling time is nearly zero if the compensation resistor R_{CMP} has the optimum value.

In a television application the value of the flyback time has to be shorter than the frame blanking time of the television standard. This is the time between the start of the frame synchronisation pulse and the start of the measuring lines of the next frame. For PAL / SECAM applications the flyback time must be shorter than 22 lines while for NTSC applications it must be shortrer than 25 lines.
Generally in monitor applications, a shorter time is needed, which depends on the standard that is used.

In the next figure, the voltage across the coil during the flyback time is simplified as a voltage jump :

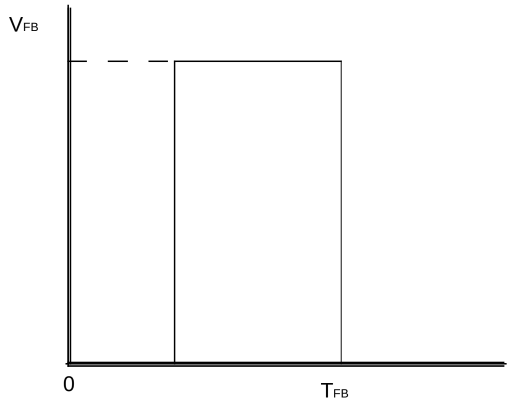


Fig 25: Simplified flyback time.

Using the simple model mentioned above, the flyback voltage V_{FB} is calculated by:

$$I_{coil(p-p)} = I_{\max} \times \left(1 - e^{-t_{FB}/x}\right)$$

where: $$I_{\max} = \frac{V_{FB}}{R_{coil(hot)} + R_M}$$ and $$x = \frac{L_{coil}}{R_{coil(hot)} + R_M}$$

$$\Leftrightarrow I_{coil(p-p)} = \frac{V_{FB}}{R_{coil(hot)} + R_M} \times \left(1 - e^{-t_{FB}/x}\right)$$

$$\Leftrightarrow I_{coil(p-p)} \times \left(R_{coil(hot)} + R_M\right) = V_{FB} \times \left(1 - e^{-t_{FB}/x}\right)$$

so : $$V_{FB} = \frac{I_{coil(p-p)} \times \left(R_{coil(hot)} + R_M\right)}{1 - e^{-t_{FB}/x}}$$

$I_{coil(p-p)}$ = coil current (peak to peak)
$R_{coil(hot)}$ = R_{coil} * 1.2 (for hot conditions at 70 °C)
R_M = measuring resistor
t_{FB} = flyback time
L_{coil} = induction of the coil

The simplified formula above, assumes that the voltage during the flyback time is constant. Actually, in an application the flyback voltage is *not* constant during the flyback time. See also paragraph 2.6 .
The influence of the damping resistor (R_{D1}) can be neglected, if it's value is about 270Ω.

Furthermore there is no need to increase the flyback voltage to compensate the spread in the line output transformer and the deflection coil, because the calculated flyback voltage is about 5% to 10 % *higher* than required and is settled when the formulae above are used.

In the next example is shown how the flyback supply voltage is calculated.
We suppose the following:

$I_{coil(p\text{-}p)}$ ≈ $I_{o(p\text{-}p)}$ = 2.4 A (the current in the damping resistor R_{D1} can be neglected if R_{D1} is not too low)
$R_{coil(hot)}$ = 6 Ω x 1.2 = 7.2 Ω
R_M = 0.5 Ω
t_{FB} = 640 µs
L_{coil} = 5 mH

then :

$$x = \frac{5\times10^{-3}}{7.2+0.5} = 649.3\times10^{-6}$$

$$V_{FB} = 2.4\times\frac{7.2+0.5}{1-e^{-640\times10^{-6}/649\times10^{-6}}} = 29.43V$$

So for the flyback supply voltage we choose 29.4 V.

2.11 Calculation of the compensation resistor R_{CMP}

The compensation resistor R_{CMP} which is mentioned in paragraph 2.7 is calculated in the following way :

$$R_{CMP} = \frac{(V_{FB} - V_{loss(FB)} - V_Z)\times R_{D1}\times R_{CV1}}{(V_{FB} - V_{loss(FB)} - I_{coil(peak)}\times R_{coil(hot)})\times R_M}$$

V_{FB} = flyback supply voltage
$V_{loss(FB)}$ = voltage loss during flyback (between pin 6 and pin 7, according specification: typical 8Volt at I_o = 1.6A)
V_Z = voltage of the external zenerdiode D4 (= equal to the value of V_P) see Fig 2: Application diagram.
R_{D1} = value of the damping resistor across the deflection coil
$I_{coil(peak)}$ = peak current through the deflection coil
$R_{coil(hot)}$ = value of the deflection coil resistance in hot condition = $R_{coil}\times 1.2$
R_M = value of the measuring resistor
R_{CV1} = value of the input resistor

example of calculating R_{CMP}:

suppose:
V_{FB} = 29.4V
$V_{loss(FB)}$ = 8V
V_Z = 14V
R_{D1} = 270Ω
$I_{coil(peak)}$ = 1.2A
$R_{coil(hot)}$ = 6Ω x 1.2 = 7.2Ω
R_M = 0.5Ω
R_{CV1} = 2.2kΩ

$$R_{CMP} = \frac{(29.4 - 8 - 14) \times 270 \times 2200}{(29.4 - 8 - 1.2 \times 7.2) \times 0.5} = 688k\Omega$$

In the formula, only the voltage loss of the flyback switch is taken into account, but there is also a small voltage loss in output stage B. To correct the calculated value that is a little bit too high, round off the value downwards by means of choosing the next lower value in the E-range. So: R_{CMP} = 680kΩ.

In Fig 26, Fig 27 and Fig 28 are some oscilloscope pictures of a 100Hz application, for different values of R_{CMP}. Pay attention to the differences in flyback time.

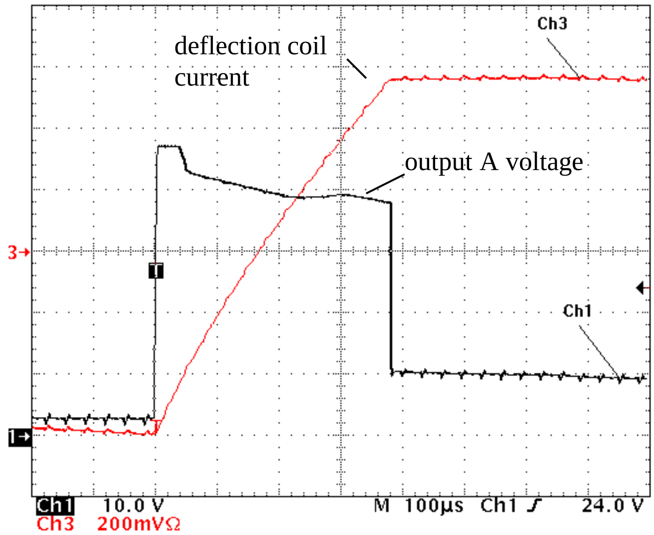


Fig 26: Correct value of R_{CMP}.

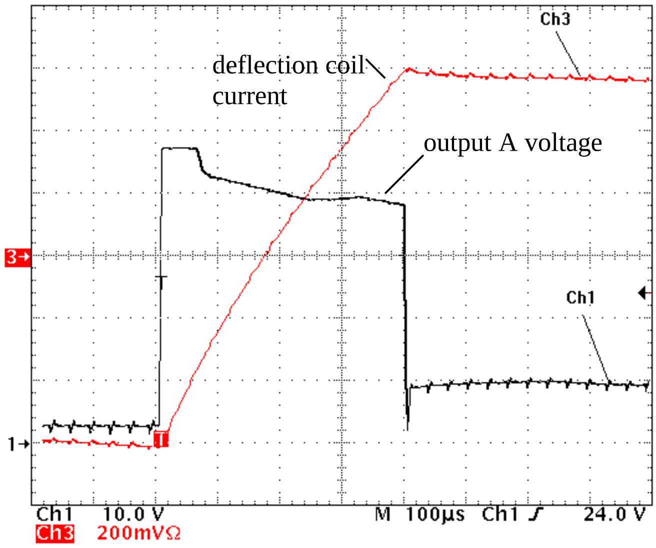


Fig 27: R_{CMP} too low, current overshoot at start scan / end flyback.

Current overshoot can be seen at the top of the picture tube as line spacing.

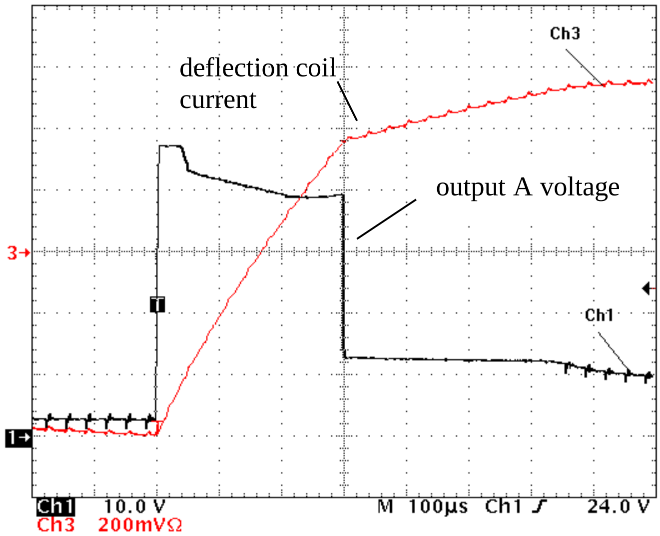


Fig 28: R_{CMP} too high, current undershoot at start scan / end flyback.

Current undershoot can be visible at the top of the picture tube as bright lines.

2.12 SOAR behaviour output

The TDA8359J is designed in a 68 volt LVDMOS (Low Voltage DMOS) process. The advantage of using MOSFETS instead of bipolar transistors for the output stage is the absence of second breakdown. Fig 29 shows the Safe Operating ARea of a bipolar transistor and of a MOSFET. It shows that the bipolar transistor delivers less current than the MOSFET, at a certain voltage. So a MOSFET output stage is more robust than a bipolar output stage. The restrictions for temperature are the same as those in the bipolar process.

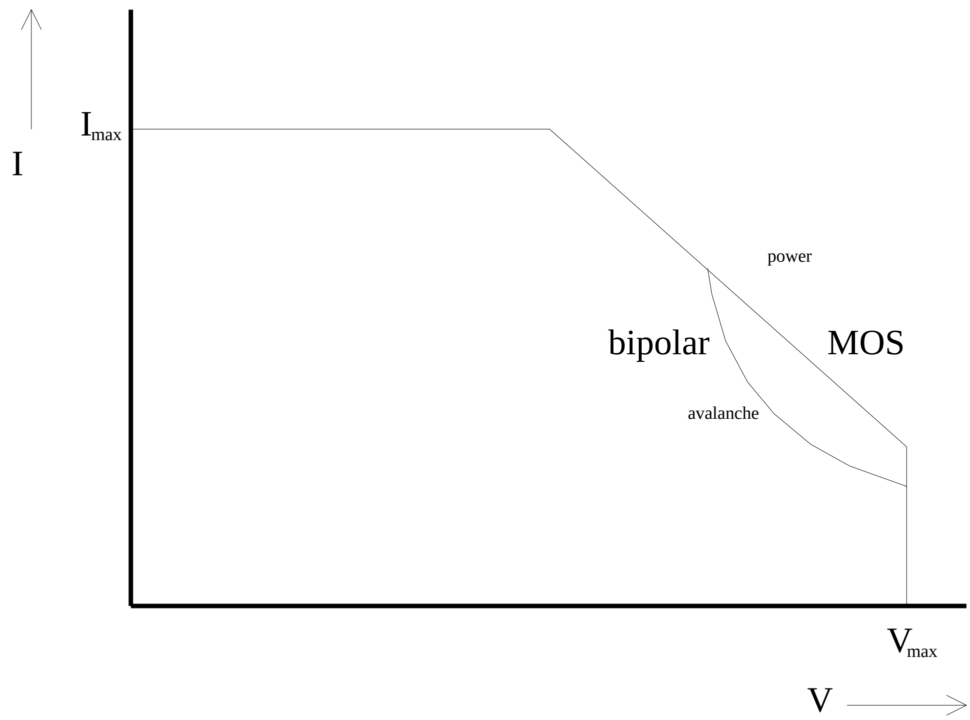


Fig 29: Power limitations.

2.13 Power dissipation of the vertical output stage

The principle diagram of the bridge output stage is given in Fig 30.

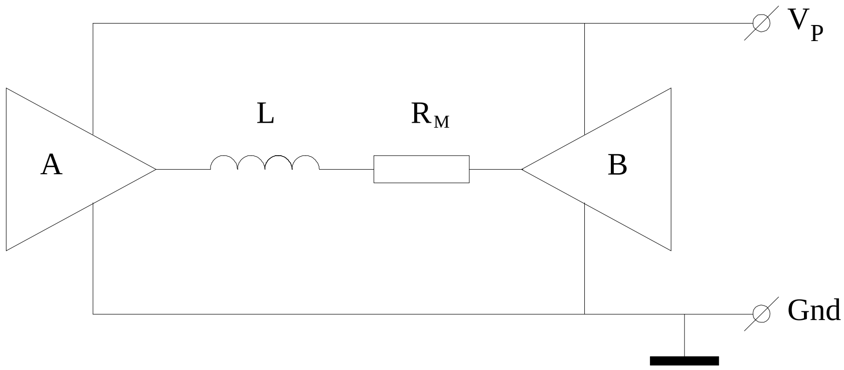


Fig 30: Principle diagram.

The total power dissipation of the TDA8359J is given by the formula:

$P_{tot}=P_{sup}-P_L$

where:

P_{sup} = Power dissipation delivered by the the supply
P_L = Power dissipation of the load that consists of $R_{coil}+R_M$

2.14 Power dissipation P_{sup}

The power dissipation that is delivered by the supply is calculated by means of the next formula:

$$P_{\sup} = \frac{V_p \times I_{\sup}}{2}$$

or $$P_{\sup} = \frac{V_p \times I_{coil(peak)}}{2}$$ because $I_{\sup} = I_{coil(peak)}$

The explanation of the formula is described, step by step, in the Appendix (paragraph 4).

The power dissipation which is caused by the quiescent current of the TDA8359J must also be taken into account:

$$V_P \times I_{q(P)(av)} = V_P \times 0.015$$

The contribution of the dissipation during the flyback time is approximately 0.3W. This is an average value for the losses in the flyback supply.

So: $$P_{\sup} = \frac{V_p \times I_{coil(peak)}}{2} + V_P \times 0.015 + 0.3$$

2.14.1 Power dissipation P_L

The power dissipation that is delivered by the load (R_{coil}+ R_M) is calculated by means of the next formula:

$$P_L = \frac{I_{coil(peak)}{}^2 \times (1.2 \times R_{coil} + R_M)}{3}$$

or $$P_L = \frac{I_{coil(p-p)}{}^2 \times (1.2 \times R_{coil} + R_M)}{12}$$

The explanation of the formula is described, step by step, in the Appendix (paragraph 4).

2.14.2 Total power dissipation P_{tot}

Eventually the total power dissipation of the TDA8359J is calculated by:

$$P_{tot} = P_{\sup} - P_L = \left[\frac{V_p \times I_{coil(peak)}}{2} + V_P \times 0.015 + 0.3\right] - \left[\frac{I_{coil(peak)}{}^2 \times (1.2 \times R_{coil} + R_M)}{3}\right]$$

example of calculating P_{tot}:

suppose:

V_P = 14V

$I_{coil(peak)}$ = 1.2A
R_{coil} = 6Ω (in cold condition)
R_M = 0.5Ω

$$P_{tot} = \left[\frac{14 \times 1.2}{2} + 14 \times 0.015 + 0.3\right] - \left[\frac{1.2^2 \times (1.2 \times 6 + 0.5)}{3}\right] = 8.91 - 3.69 = 5.22W$$

2.15 Heatsink calculation

The value of the heatsink can be calculated in a standard way with a method based on average temperatures. The heatsink must be chosen in such a way that the temperature of the die does not exceed the maximum allowable temperature of 150°C, as specified in the device specification.
However, in general we recommend to design for an average die temperature that does not exceed 130°C.

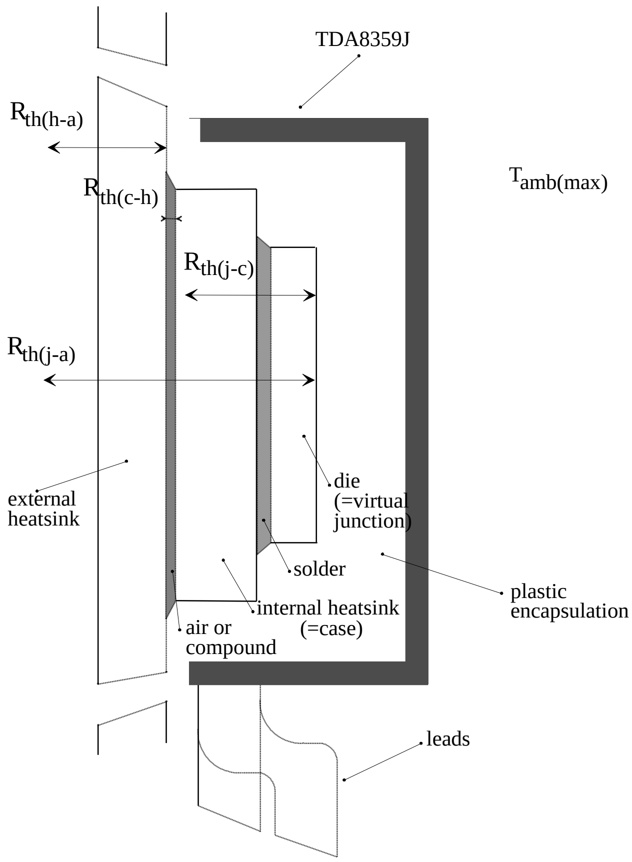


Fig 31: Construction of the TDA8359J mounted on a heatsink.

The construction of the TDA8359J mounted on a heatsink is drawn in Fig 31. In this picture one can see several thermal resistances:

$R_{th(h-a)}$ = thermal resistance between heatsink and the ambient
$R_{th(c-h)}$ = thermal resistance between case and heatsink
$R_{th(j-c)}$ = thermal resistance between die (junction) and case
$R_{th(j-a)}$ = thermal resistance between die and ambient
$T_{amb(max)}$ = maximum ambient temperature
P_{tot} = total power dissipation of the TDA8359J

The thermal resistance $R_{th(j-a)}$ between the die and ambient is calculated by means of the next formulae:

$$R_{th(j-a)} = R_{th(j-c)} + R_{th(c-h)} + R_{th(h-a)} \quad \text{and} \quad T_j - T_{amb} = P_{tot} \times R_{th(j-a)}$$

$$\Leftrightarrow T_j - T_{amb} = P_{tot} \times \left(R_{th(j-c)} + R_{th(c-h)} + R_{th(h-a)}\right)$$

$$\Leftrightarrow R_{th(h-a)} = \frac{T_j - T_{amb}}{P_{tot}} - \left(R_{th(j-c)} + R_{th(c-h)}\right)$$

T_j = temperature of the junction (die)
T_{amb} = temperature of the ambient

The heatsink temperature T_h will be:

$$T_h = T_{amb} + \left(R_{th(h-a)} \times P_{tot}\right)$$

example of calculating $R_{th(h-a)}$:

suppose:
T_j = 120 °C (We recommend this for a safe value)
T_{amb} = 40 °C
P_{tot} = 6 Watt
$R_{th(j-c)}$ = 4 K/W
$R_{th(c-h)}$ = 2 K/W

$$R_{th(h-a)} = \frac{120-40}{6} - (4+2) = 7.3K/W$$

The heatsink temperature will be:

$$T_h = 40 + (7.3 \times 6) = 83.8\ °C$$

It may be clear that, to *decrease* the temperature of the heatsink or the allowed temperature inside the cabinet, the dimensions of the heatsink should be *increased.*

2.16 Heatsink mounting

There is a direct electrical connection between the mounting base and the ground pin of the TDA8359J. The die is soldered on the internal heatsink, see also Fig 31. The heatsink can be connected to ground to achieve a better EMC behaviour.

The thermal resistance between case and heatsink $R_{th(c-h)}$ depends on the mounting method of the TDA8359J on the heatsink. This can be clip or screw mounting. Both mounting methods can give acceptable results, if the instructions are followed. In general, screw mounting will result in lower $R_{th(c-h)}$ values than clip mounting. The main reason is the difference in press on force of the power encapsulation case to the heatsink.

Insulation between the case and heatsink can also be used, however this is not recommended. When insulation is used, the $R_{th(c-h)}$ has a higher value.

A table is given below that shows the influence of the torque on the kappa value $R_{th(c-h)}$ with screw and clip mounting. The table clearly shows the difference in kappa value for dry mounting, mounting with heatsink compound and mounting with insulation.

torque (Ncm)	heatsink compound (K/W)		dry (K/W)		with insulation (K/W)	
	screw	clip	screw	clip	screw	clip
10	-	1.25	-	4.26	-	6.25
20	0.92	1.23	2.46	4.07	3.60	5.96
30	0.90	1.22	2.37	3.85	3.51	5.69
40	0.87	1.21	2.27	3.66	3.42	5.53
50	0.85	1.19	2.22	3.53	3.41	5.35
60	0.83	1.18	2.16	3.40	3.40	5.18
100	-	1.14	-	3.05	-	4.78

2.17 Flash precautions

To minimize the risk of damage to the device due to flashover in the picture tube, pay attention of a proper design of grounding.

- First connect the aquadag layer to the ground of the picture tube on the printed circuit board which is mounted on the picture tube, and then to the ground near the horizontal output transformer.
- The use of ferroxcube core beads around the deflection coil wires gives extra protection.
- Furthermore use a RC filter between OUTA (pin7) and ground (pin5), *as close as possible to the pins* of the TDA8359J. The value of the filter is 1.5Ω and 47nF to 150nF.

More information about flashover can be found in the report “Application information for flashover protection of vertical deflection TDA8359J”

2.18 EMC behaviour

When problems are found around the EMC behaviour of the application, the problems should be split into:

1. Susceptibility problem (radiation coming from outside of the IC).
2. Radiation problem (coming from the IC itself).

In both cases it is important to know what the frequency is that causes the problem(s).

Recommendations:

Reduction of the susceptibility and radiation can be achieved by:

- limit the bandwidth of the system.
- keep loop areas small to reduce magnetic pick up.
- keep sensitive tracks short to reduce electrical pick up.

A. **Bandwidth of the noise**
The bandwidth can be limited by filtering the input, output and power supply. Pay attention to small loop areas and short tracks during the design of the layout of the printed circuit board.

B. **Drive signal**
The drive signal tracks from the drive circuit to the TDA8359J should be routed close to each other and made as short as possible. This is to minimize the loop area.
To supress (EMC) interference it is possible to insert a series resistor of 100Ω – 1kΩ in the drive signals close to the driver. Furthermore capacitors on the pins of the driver of about 560pF – 1nF.

C. **Decoupling capacitors**
In general, the use of small decoupling capacitors of 2.2 nF between the input pins and ground will solve problems at the input side. The capacitors must be connected directly to ground (pin 5) of the TDA8359J. This has to be done with short wires and tracks in order to minimize parasitic inductance.

D. **Power supplies**
It is recommended to decouple the power supplies locally and as close as possible to the TDA8359J. Especially the high frequency decoupling capacitor must be connected as close as possible to the pins of the IC. The main power supply and the flyback power supply, should be both decoupled with 100nF capacitors.

E. **Deflection coil**
The connection to the deflection coil is usual done with relatively long wires. These ‘long’ wires behave as an aerial which picks up RF disturbances. If two blocking inductors of 2 µH are placed in these wires, a good blocking of the disturbance is achieved. The inductors can be implemented as a "bead on wire".

F. **Heatsink**
For good EMC behaviour the heatsink should be grounded and not left electrically floating. The copper backside of TDA8359J is soldered to the backside of the crystal and is *electrically connected to the groundpin (pin 5)*.

G. Circuit
For optimal suppression, the circuit in Fig 32 can be used as guidance.

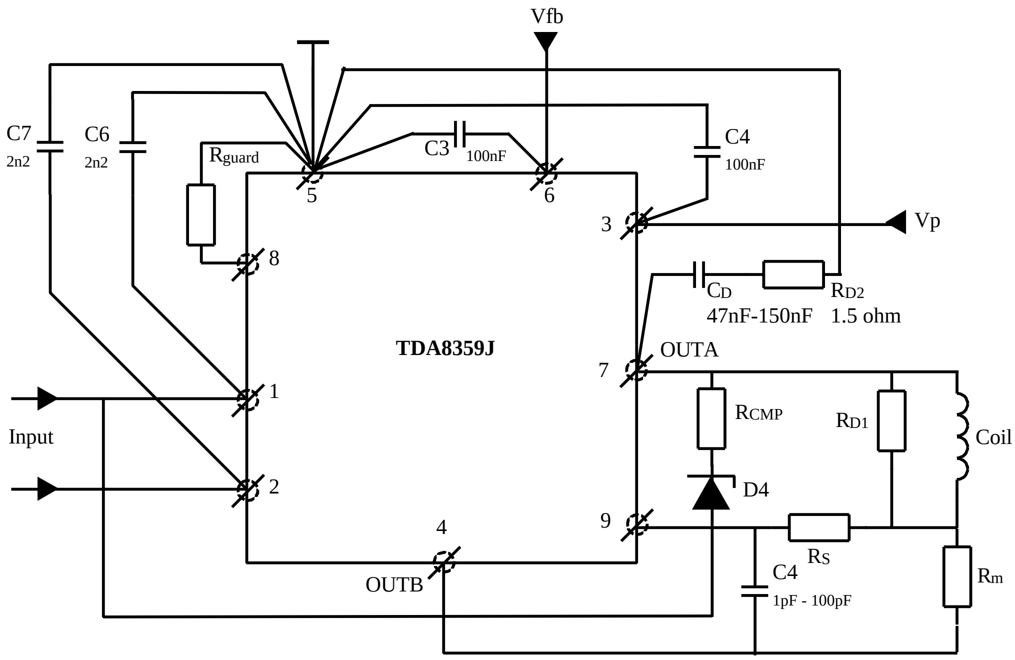


Fig 32: Recommended application for optimal suppression.

2.19 Application design procedure of the TDA8359J

Below are some remarks on practical applications. Designers will know most of them.

For the design-in of TDA8359J it is advised to use the following design steps:

1. Read the minimum, typical and the maximum vertical deflection current from the picture tube coil specification. The output current of the TDA8359J (I_{coil}) should not exceed the maximum vertical deflection current (according the value in the specification).

2. Calculate the main- and flyback supply voltage. It should be as low as possible to avoid high dissipation, but pay attention to the spread in the used EHT transformers. See paragraph 2.10.

3. Calculate the value of the conversion resistors (R_{cv1} and R_{cv2}) and measurement resistor (R_M). Be aware that the typical bias input voltage of the TDA8359J is 880 mV, minimum bias voltage is 300 mV (for linearity) and the maximum bias voltage is 1600 mV. The typical differential input voltage is 1000 mV(p-p) with a maximum of 1500 mV(p-p). See paragraph 2.3.2 above.

4. Choose the damping resistor (R_{D1}) about 300 Ω (R_{D1} is dependent of the picture tube coil and should be as high as possible) and calculate the value of the compensation resistor R_{CMP}, see paragraph 2.11. In general a too low compensation resistor value results in overshoot and a too high value results in undershoot. A proper compensation resistor value does not cause over- or undershoot. See also paragraph 2.11.

5. Choose R_s about 2.7kΩ. The value for R_s should have at least the value of the input resistors $R_{cv1,2}$ and at most two times $R_{cv1,2}$. See paragraph 2.4.1. Eventual, a small capacitor of 1pF - 100pF can be placed between pin 9 (FEEDB) and pin 4 (OUTB) to supress minor oscillations.

6. Calculate the heatsink. See paragraph 2.15.

7. For connecting the vertical guard, see paragraph 2.9.1.

8. Good HF decoupling of both supplies (pin 3 and 6) is necessary. The use of a 100nF foil capacitor (not a SMD) which is mounted as close as possible to both power supply pins and to ground is strongly recommended, to reduce PCB-track inductance during a flashover in the picture tube.

9. Connect the load capacitors from the supplies to the same ground as the TDA8359J (pin5), to assure a better flash behaviour. Recommended values are 220µF at pin 3 (V_P) and 47µF at pin 6 (V_{FB}).

10. Optional: For flashover precaution it is strongly recommended to connect a RC filter between OUTA (pin 7) and ground (pin 5) that consists of 1.5Ω in series with 47nF to 150 nF and should be connected as close as possible to the pins of the TDA8359J. For more information about flashover see the report “Application information for flashover protection of vertical deflection TDA835X”.

11. Pay attention to the symmetry of the tracks to the input pins (pin 1 and 2). Long tracks should be avoided. The use of decoupling capacitors between the input pins and ground minimizes the interference susceptibility. Both decoupling capacitors must have the same value and should be placed close to pin 1 and pin 2, just like the input resistors. If the value of these capacitors is too high, minor oscillations *could* occur at the start- or end of the scan. The recommended value is 2.2nF.

3. APPLICATION INVESTIGATION

3.1 Introduction

A more detailed investigation may be required, depending on the application. Whether such an investigation is necessary can be determined by comparing the actual application with the figures in the next paragraphs.

3.2 Power peak at the start and end of flyback

When an RC-filter is used between OUTA and GND in an application with the TDA8359J, a current peak at the end of the flyback could arise. In the next cases one can see that these current peaks *don't damage* the TDA8359J.

3.2.1 Application without RC filter

In Fig 33 the voltage of OUTA (pin 7), the current of OUTA (pin 7) and the current of GND (pin 5) is measured in an application *without* RC-filter

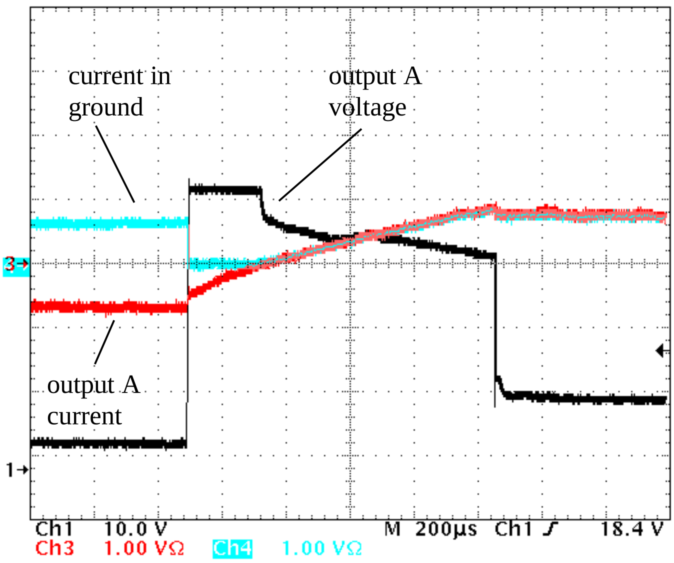


Fig 33: Flyback time of application without RC-filter on OUTA

In Fig 34 is the begin of the flyback stretched out while in Fig 35 the end of the flyback is stretched out.

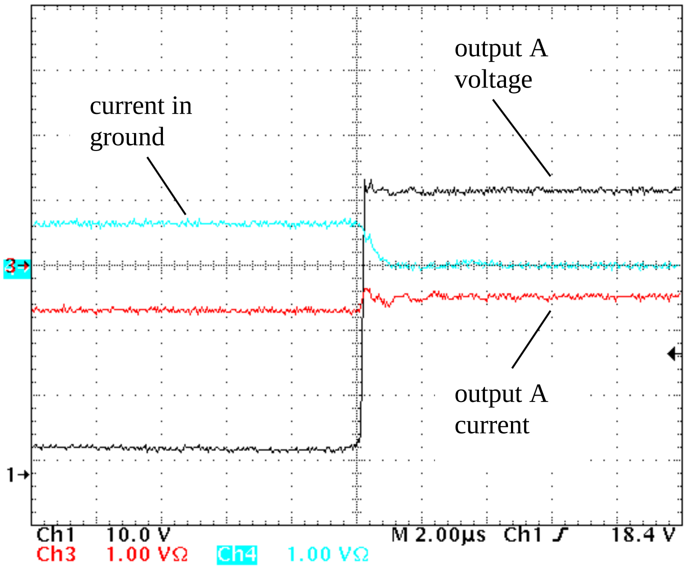


Fig 34: Flyback time of application without RC-filter on OUTA.

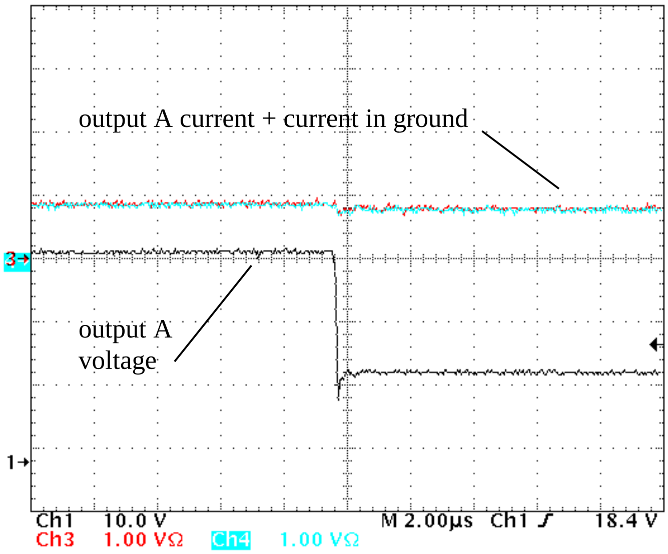


Fig 35: Flyback time of application without RC-filter on OUTA.

As can be seen in Fig 34 and in Fig 35, there are no current peaks at output A or ground at the start- and end of the flyback. The small step in the output A current is the current that flows through the damping resistor.

3.2.2 Application with RC-filter 47 nF + 1.5 Ohm

When a low ohmic RC-filter (47 nF + 1.5 Ohm) is used between OUTA and ground for flash protection, a peak current occurs at OUTA and GND at the end of the flyback. See Fig 36 and Fig 37.

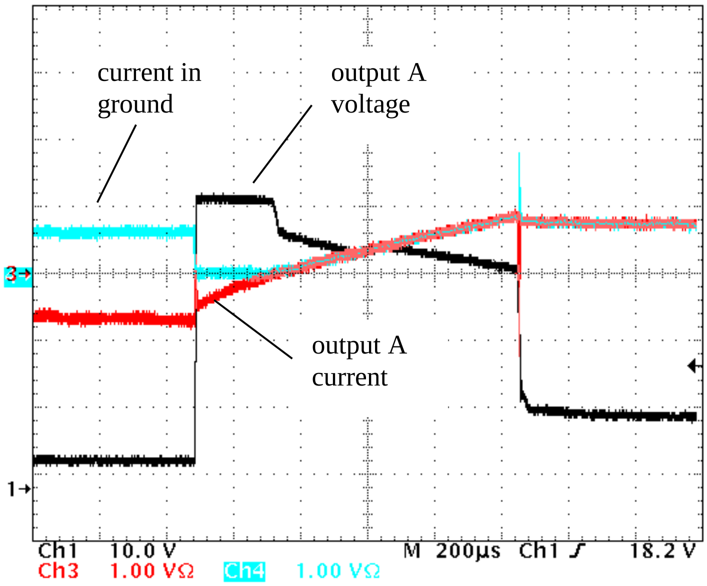


Fig 36: Application with RC-filter between OUTA and ground (47 nF + 1.5 Ohm).

In Fig 37 the begin of the flyback is stretched out while in Fig 38 the end of the flyback is stretched out.

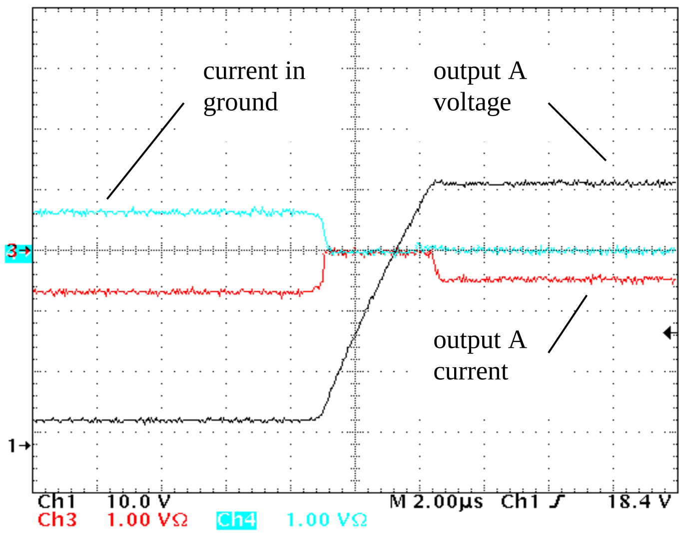


Fig 37: Application with RC-filter between OUTA and ground (47 nF + 1.5 Ohm).

As can be seen in Fig 37 the rise time of the flyback pulse increases when an RC-filter on OUTA is used. This has no influence on the performance of the TDA8359J. During the rise time of the flyback, the current of pin OUTA is zero. This is due to charging the capacitor of the RC-filter. Then the current from the deflection coil flows in the capacitor of the RC-filter.

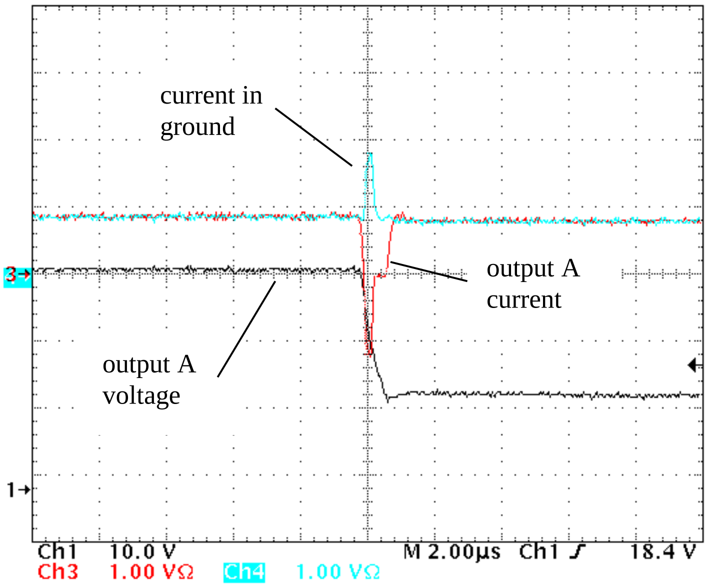


Fig 38: Application with RC-filter between OUTA and ground (47 nF + 1.5 Ohm).

As can be seen in Fig 38 a current peak of 1.8 A occurs in the GND pin at the end of the flyback. Also a negative current peak of 1.2 A occurs in the OUTA at the end of the flyback. These peaks are due to discharge of the capacitor of the RC-filter. The discharge current of the capacitor flows via the bottom transistor of the A-output of TDA8359J to GND. See Fig 39. Because the time of these peaks are *very short*, this will cause *no damage* to the TDA8359J.

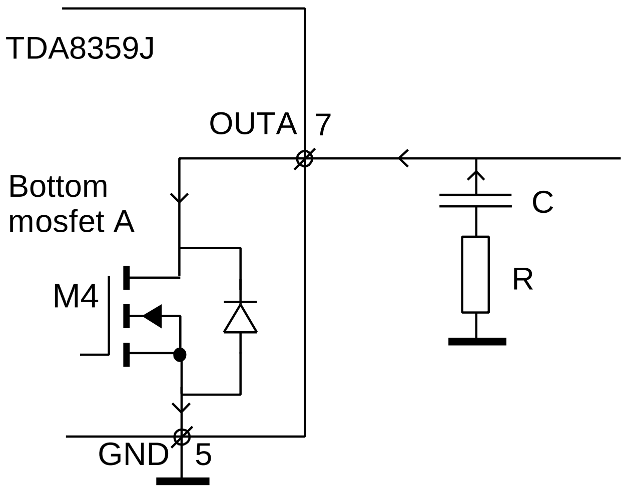


Fig 39: TDA8359J , current flow when discharging C.

3.2.3 Application with RC-filter 150 nF + 1.5 Ohm

When a low ohmic RC-filter with an even higher capacitor is used (150 nF), higher current peaks occur in OUTA and GND at the end of flyback. See Fig 40 and Fig 41.

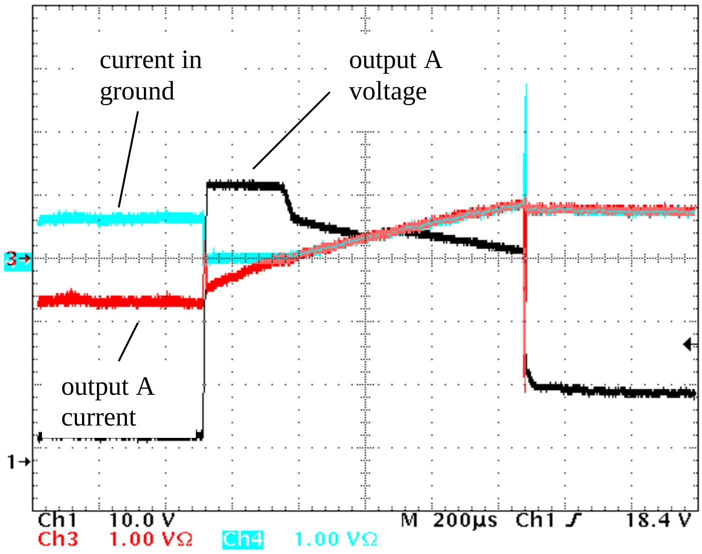


Fig 40: Application with RC-filter on OUTA (150 nF + 1.5 Ohm).

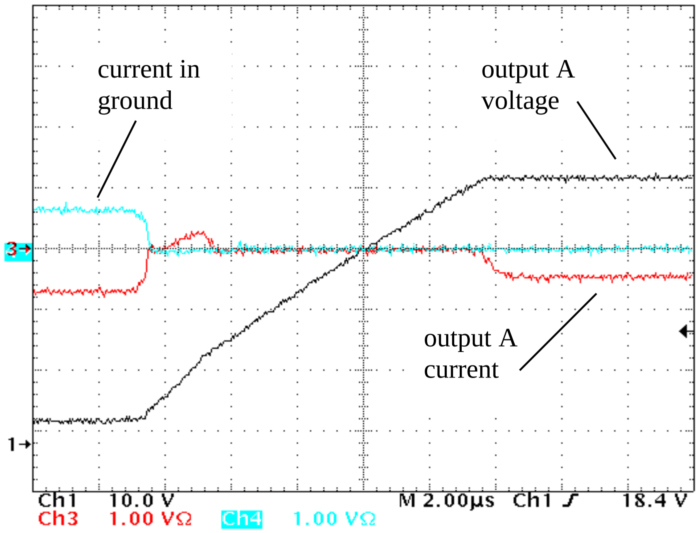


Fig 41: Application with RC-filter on OUTA (150 nF + 1.5 Ohm).

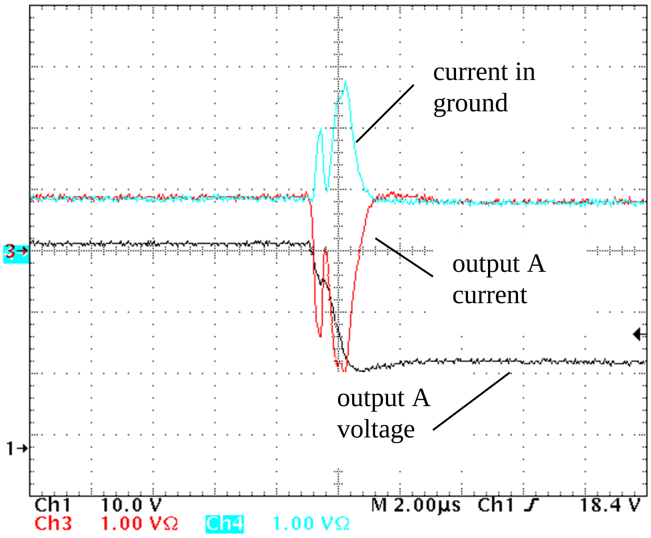


Fig 42: Application with RC-filter on OUTA (150 nF + 1.5 Ohm).

As can be seen in figure 39 the rise (and also fall) time of the flyback pulse increases when a RC-filter on OUTA with a capacitor of 150nF is used. This also has no influence on the performance of the TDA8359J. During the rise time of the flyback, the current of pin OUTA is zero. This is due to charging the capacitor of the RC-filter. Then the current from the deflection coil flows in the capacitor of the RC-filter.

As can be seen in figure 41, a current peak of 2.8 A occurs in the GND at the end of the flyback. Also a negative current peak of 2A occurs in the OUTA during fall time of flyback. These peaks are due to discharge of the capacitor of the RC-filter. The discharge current flows via the bottom transistor of the A-output of TDA8359J to GND. See figure 38.
And again, also in this case, there is *no damage* of the TDA8359J because the time of the current peak is *very short*.

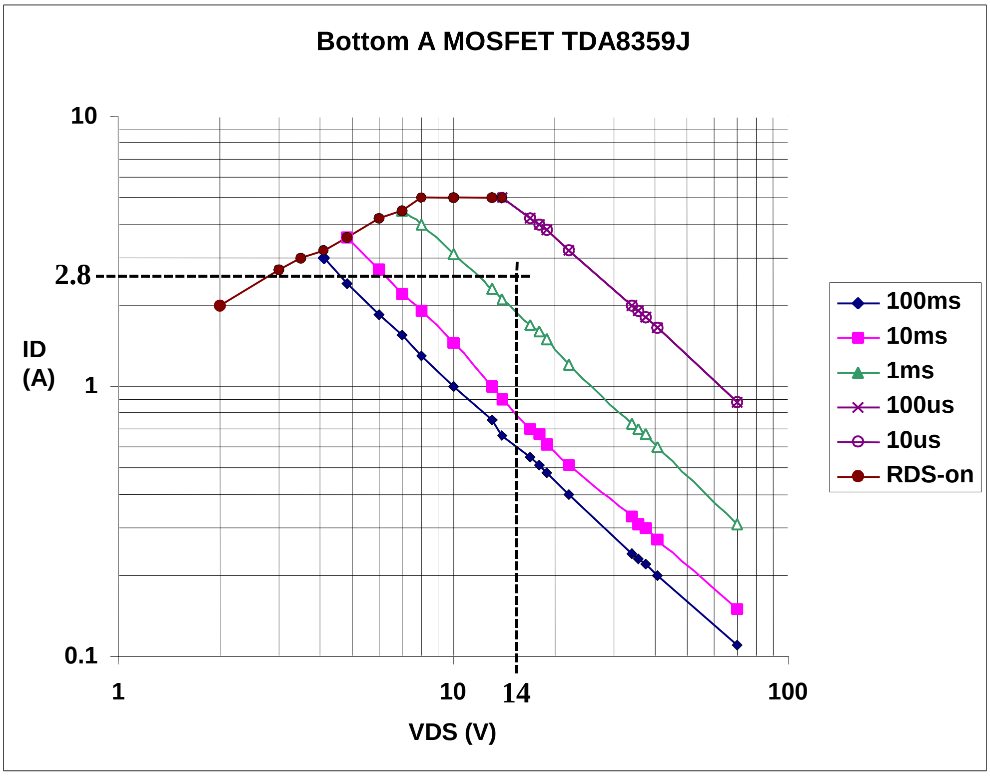


Fig 43: SOAR Bottom A MOSFET TDA8359J.

The above figure shows the current that is allowed for the bottom transistor A at a certain voltage and time duration. It is established by infrared equipment.
The bottom transistor A is pulse controlled in such a way that it is conducting while the temperature of this transistor does not exceed 200 °C.
The allowed value of the current and voltage increases when the pulse duration decreases.

So, as one can see the current peak in Fig 42 does not damage the TDA8359J, the time duration of the small current peak < 2 µS while the current is 2.8A and the voltage is 14V.

4. APPENDIX

4.1 Calculating the power dissipation P_{sup}

The powerdissipation that is delivered by the supply is calculated in the following way:

The current (I_{sup}) that is delivered by the power supply during the scan time is illustrated in the figure below.

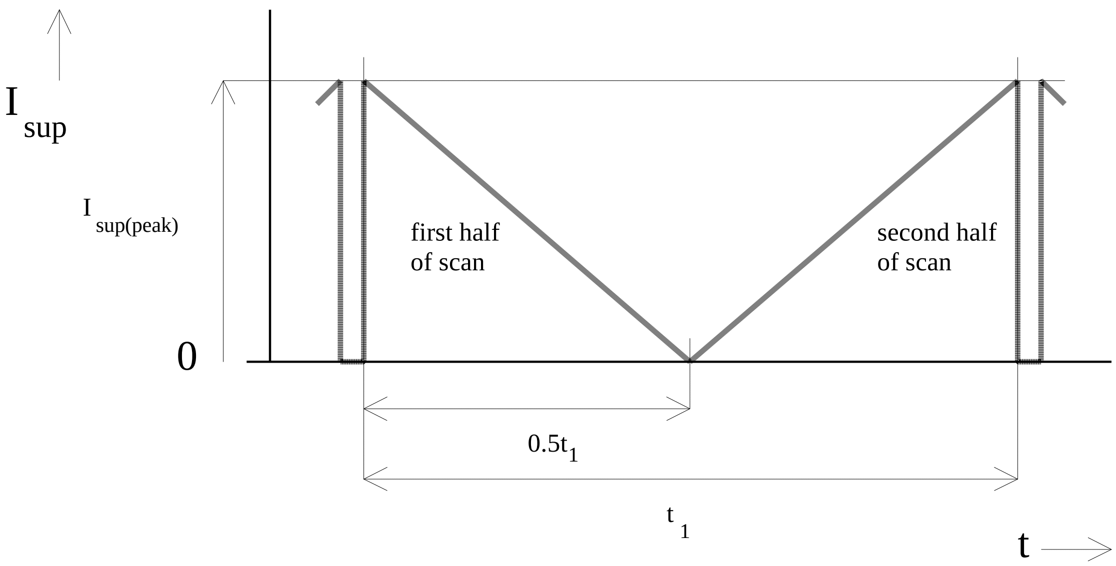


Fig 44: Current of the supply.

The *momentary* supply current I_{sup} is expressed by the formula:

for $0 \le t \le 0.5t_1$ (first half of the scan):

$$I_{sup}(t) = I_{sup(peak)} - \left(2 \times I_{sup(peak)} \times \frac{t}{t_1}\right)$$

$$\Leftrightarrow I_{sup}(t) = I_{sup(peak)} \times \left(1 - 2 \times \frac{t}{t_1}\right)$$

for $0.5t \le t \le t_1$ (second half of the scan):

$$I_{sup}(t) = \left(2 \times I_{sup(peak)} \times \frac{t}{t_1}\right) - I_{sup(peak)}$$

$$\Leftrightarrow I_{sup}(t) = I_{sup(peak)} \times \left(2 \times \frac{t}{t_1} - 1\right)$$

Because of the symmetry for the first- and the second half of the power supply, the *average* power delivered by the supply is:

$$P_{\sup} = 2 \times \frac{1}{t_1} \times \int_0^{0.5t_1} \left(V_p \times I_{\sup} - 2 \times V_p \times I_{\sup} \times \frac{t}{t_1} \right) dt$$

$$\Leftrightarrow P_{\sup} = \frac{2}{t_1} \times \int_0^{0.5t_1} V_p \times I_{\sup} \times \left(1 - 2 \times \frac{t}{t_1} \right) dt$$

$$\Leftrightarrow P_{\sup} = \frac{2 \times V_p \times I_{\sup}}{t_1} \times \int_0^{0.5t_1} \left(1 - 2 \times \frac{t}{t_1} \right) dt$$

$$\Leftrightarrow P_{\sup} = \frac{2 \times V_p \times I_{\sup}}{t_1} \times \left[t - \frac{t^2}{t_1} \right]_0^{0.5t_1}$$

$$\Leftrightarrow P_{\sup} = \frac{2 \times V_p \times I_{\sup}}{t_1} \times \frac{1}{4} \times t_1$$

$$\Leftrightarrow P_{\sup} = \frac{V_p \times I_{\sup}}{2}$$

or $P_{\sup} = \dfrac{V_p \times I_{coil(peak)}}{2}$ because $I_{\sup} = I_{coil(peak)}$

4.2 Calculating the power dissipation P_L

The power dissipation in the load (R_{coil}+R_M) is calculated in the following way:

The current through the deflection coil I_{coil} and the current through the measurement resistor R_M are equal and can be seen in Fig 45.

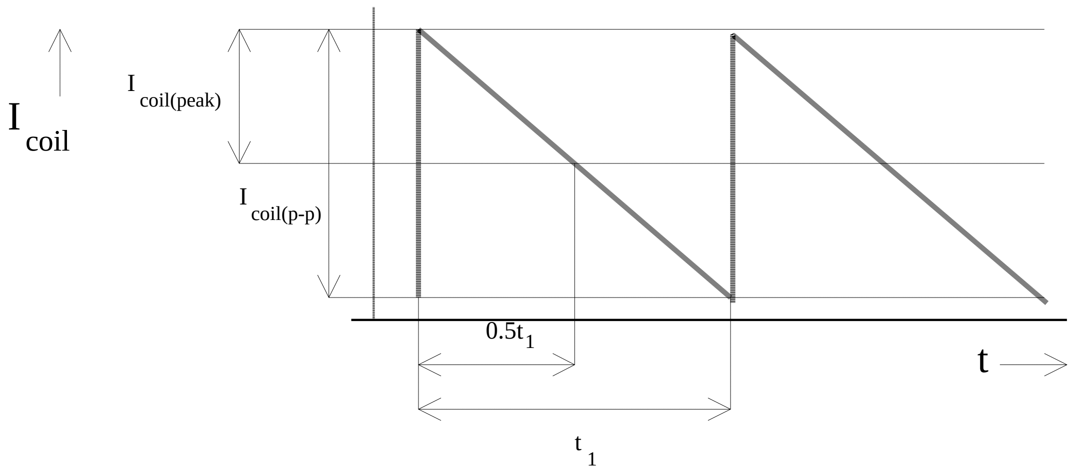


Fig 45: Current through the deflection coil and R_M.

The *momentary* current in the deflection coil is given by:

$$I_{coil}(t) = I_{coil(peak)} - \left(2 \times I_{coil(peak)} \times \frac{t}{t_1}\right)$$

$$\Leftrightarrow I_{coil}(t) = I_{coil(peak)} \times \left(1 - 2 \times \frac{t}{t_1}\right)$$

The *momentary* dissipated power $P_L(t)$ in the load (R_{coil} + R_M):

since: $P = I^2 \times R$

$$\Leftrightarrow P_L(t) = I_{coil(peak)}{}^2 \times \left(1 - 2 \times \frac{t}{t_1}\right)^2 \times (R_{coil} + R_M)$$

Because of the symmetry of the first- and the second half of the current through the load, the *average* power dissipation in the load is:

$$P_L = \frac{2}{t_1} \times \int_0^{0.5t_1} \left(I_{coil(peak)}\right)^2 \times \left(1 - 2 \times \frac{t}{t_1}\right)^2 \times \left(R_{coil} + R_M\right) dt$$

$$\Leftrightarrow P_L = \frac{2 \times \left(I_{coil(peak)}\right)^2 \times \left(R_{coil} + R_M\right)}{t_1} \times \int_0^{0.5t_1} \left(1 - 2 \times \frac{t}{t_1}\right)^2 dt$$

$$\Leftrightarrow P_L = \frac{2 \times \left(I_{coil(peak)}\right)^2 \times \left(R_{coil} + R_M\right)}{t_1} \times \int_0^{0.5t_1} \left(1 - 4 \times \frac{t}{t_1} + 4 \frac{t^2}{t_1^2}\right) dt$$

$$\Leftrightarrow P_L = \frac{2 \times \left(I_{coil(peak)}\right)^2 \times \left(R_{coil} + R_M\right)}{t_1} \times \left[t - \frac{4}{2} \cdot \frac{t^2}{t_1} + \frac{4}{3} \cdot \frac{t^3}{t_1^2} \right]_0^{0.5t_1}$$

$$\Leftrightarrow P_L = \frac{2 \times \left(I_{coil(peak)}\right)^2 \times \left(R_{coil} + R_M\right)}{t_1} \times \left[0.5 \cdot t_1 - 2 \cdot \frac{(0.5 \cdot t_1)^2}{t_1} + \frac{4}{3} \cdot \frac{(0.5 \cdot t_1)^3}{t_1^2} \right]$$

$$\Leftrightarrow P_L = \frac{2 \times \left(I_{coil(peak)}\right)^2 \times \left(R_{coil} + R_M\right)}{t_1} \times \left[\frac{1}{2} \cdot t_1 - \frac{1}{2} \cdot t_1 + \frac{1}{6} \cdot t_1 \right]$$

$$\Leftrightarrow P_L = \frac{2 \times \left(I_{coil(peak)}\right)^2 \times \left(R_{coil} + R_M\right)}{t_1} \times \frac{1}{6} \cdot t_1$$

$$\Leftrightarrow P_L = \frac{{I_{coil(peak)}}^2 \times \left(R_{coil} + R_M\right)}{3}$$

or $$P_L = \frac{{I_{coil(p-p)}}^2 \times \left(R_{coil} + R_M\right)}{12}$$ because $I_{coil(p-p)} = 2 \times I_{coil(peak)}$

For calculations the coil resistance is multiplied by 1.2 for hot conditions of the deflection coil

$$P_L = \frac{I_{coil(peak)}^{\;2} \times (1.2 \times R_{coil} + R_M)}{3}$$

or

$$P_L = \frac{I_{coil(p-p)}^{\;2} \times (1.2 \times R_{coil} + R_M)}{12}$$

5. REFERENCES

- Application note TDA8358J (AN99009)
- Application note TDA935X/6X/8X (AN98093)
- Application note TDA884X/885X-N2 (AN98002)

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